The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

Supplement to The TTL Data Book

for Design Engineers

Second Edition

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IMPORTANT NOTICES

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Information contained herein is supplemental to the date published in LCC4112.

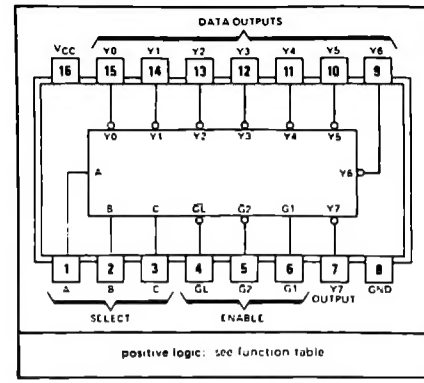
TABLE OF CONTENTS

TO BE ANNOUNCED

TYPES SN54LS137, SN74LS137 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

NOVEMBER 1977

SN54LS137 . . . J OR W PACKAGE
SN74LS137 . . . J OR N PACKAGE
(TOP VIEW)

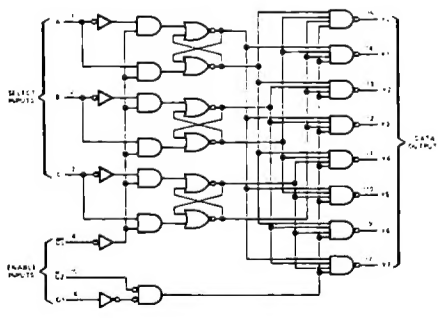


- Combines Decoder and 3-Bit Address Latch
- Incorporates 3 Enable Inputs to Simplify Cascading
- Low Power Dissipation . . . 65 mW Typ

description

The 'LS137 is a three-line to eight-line decoder demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'LS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The 'LS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

functional block diagram



FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant

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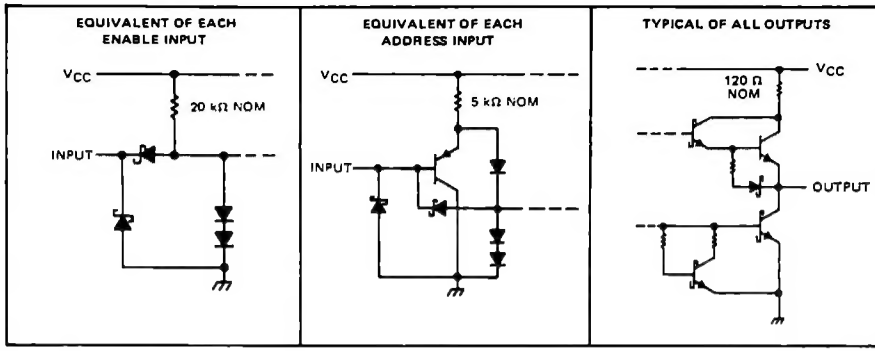
schematics of inputs and outputs



TYPICAL APPLICATION DATA

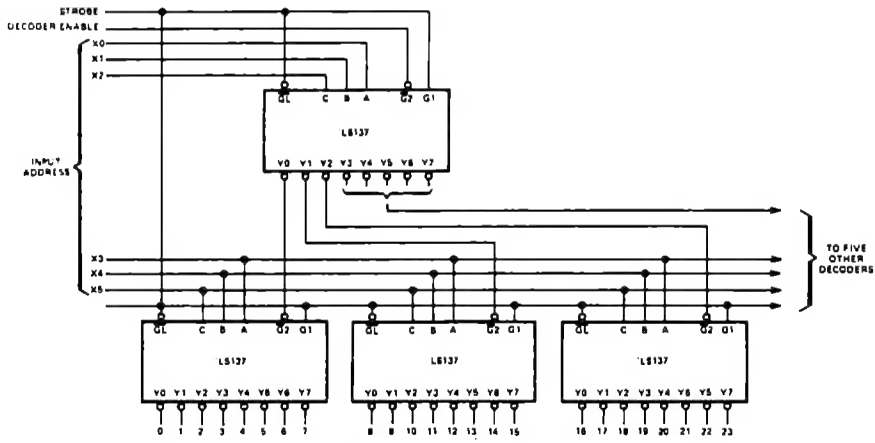


FIGURE 1–6-LINE TO 64-LINE DECODER WITH INPUT ADDRESS STORAGE

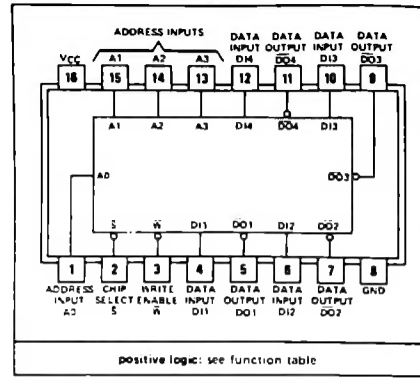
TO BE ANNOUNCED

TYPES SN54LS189, SN54LS219, SN54LS289, SN54LS319, SN74LS189, SN74LS219, SN74LS289, SN74LS319 64-BIT RANDOM-ACCESS READ/WRITE MEMORIES

NOVEMBER 1977

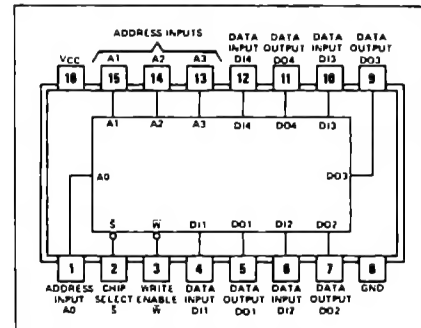
- Organized as 16 Words of Four Bits Each
- Schottky-Clamped for High Performance
- Full On-Chip Decoding and Fast Chip-Enable Simplify System Decoding
- P-N-P Inputs Reduce Loading on System Buffers/Drivers
- Choice of 3-State or Open-Collector Outputs
- Choice of True or Inverted Outputs

SN54LS189, SN54LS289 . . . J OR W PACKAGE
SN74LS189, SN74LS289 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS219, SN54LS319 . . . J OR W PACKAGE
SN74LS219, SN74LS319 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic TTL memories feature Schottky clamping for high performance and a fast chip-select access time to enhance decoding at the system level. A three-state-output version and an open-collector-output version are offered for both of the logic choices. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.

write cycle

Information to be stored in the memory is written into the selected address (AD) location when the chip-select ($\overline{S}$) and the write-enable ($\overline{W}$) inputs are low. While the write-enable input is low, the memory outputs are off (three-state = Hi-Z, open-collector = high). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

read cycle

Information stored in the memory (see function table for input/output phase relationship) is available at the outputs when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the outputs will be off.

FUNCTION TABLE

FUNCTION	INPUTS		OUTPUTS			
	CHIP SELECT	WRITE ENABLE	'LS189	'LS289	'LS219	'LS319
Write	L	L	Z	Off	Z	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered	Data Entered	Data Entered
Inhibit	H	X	Z	Off	Z	Off

H = high level, L = low level, X = irrelevant, Z = high impedance

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TYPES SN54LS320, SN54LS321, SN74LS320, SN74LS321 CRYSTAL-CONTROLLED OSCILLATOR

NOVEMBER 1977

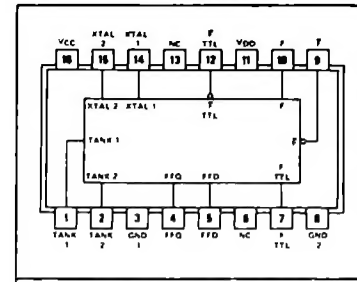
'LS320

- Crystal-Controlled Oscillator Operation from 1 Hz to 20 MHz
- High-Level 2-Phase Outputs
- TTL-Level 2-Phase Outputs

'LS321

- Similar to 'LS320 But Includes f/2 and f/4 TTL-Level Count-Down Outputs

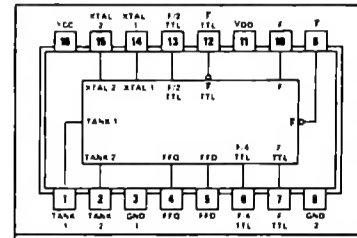
SN54LS320 . . . J OR W PACKAGE
SN74LS320 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description

NC—No internal connection

SN54LS321 . . . J OR W PACKAGE
SN74LS321 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description

description

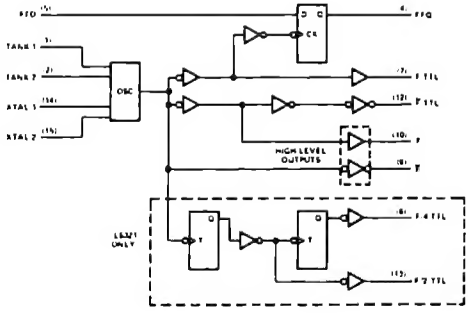
The 'LS320 is a crystal-controlled oscillator/clock driver. It features complementary TTL-Level (5-volt) and high-level (5- to 12-volt) outputs.

The high-level outputs are very-low-impedance devices and can be used with V_{DD} at 5 volts to drive highly capacitive TTL-level lines. If the high-level outputs are not used, then the V_{DD} terminal can be left open. A synchronization flip-flop is included.

The 'LS321 is identical to the 'LS320 except it also features two TTL-level count-down outputs, f/2 and f/4.

The SN54LS320 and SN54LS321 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS320 and SN74LS321 will be characterized for operation from 0°C to 70°C.

functional block diagram



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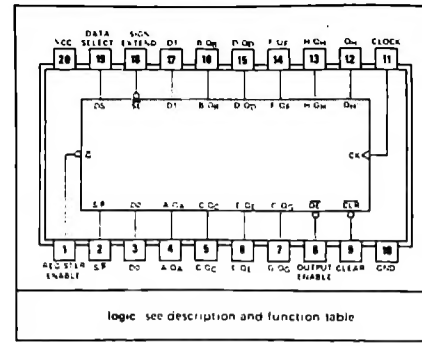
TYPES SN54LS322, SN74LS322
8-BIT SHIFT REGISTERS WITH SIGN EXTEND

BULLETIN NO. DL-S 12587, OCTOBER 1977

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- 3-State Outputs Drive Bus Lines Directly
- Sign Extend Function
- Direct Overriding Clear

SN54LS322 . . . . J PACKAGE
SN74LS322 . . . . J OR N PACKAGE
(TOP VIEW)



logic see description and function table

description

These low-power Schottky eight-bit shift registers feature multiplexed input/output data ports to achieve full eight-bit data handling in a single 20-pin package. Serial data may be entered into the shift-right register through either the D0 or the D1 input as selected by the data select input. A serial output (Q_H') is also provided to facilitate expansion. Synchronous parallel loading is accomplished by taking both the register enable and the $S/\overline{P}$ inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high transition of the clock. The data extend function repeats the sign in the Q_A flip-flop during shifting. A direct overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not interfere with synchronous operation of the register.

FUNCTION TABLE

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT
	CLEAR	REGISTER ENABLE	$S/\overline{P}$	SIGN EXTEND	DATA SELECT	OUTPUT ENABLE	CLOCK	A/Q_A	B/Q_B	C/Q_C . . . H/Q_H		Q_H'
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}	Q_{H0}
Shift Right	H	L	H	H	L	L	↑	D0	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
	H	L	H	H	H	L	↑	D1	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Sign Extend	H	L	H	L	X	L	↑	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state. However, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0} . . . Q_{H0} = the level of Q_A through Q_H, respectively, before the indicated steady state conditions were established
Q_{An} . . . Q_{Hn} = the level of Q_A through Q_H, respectively, before the most recent ↑ transition of the clock
D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively
a . . . h = the level of steady-state inputs at inputs A through H respectively

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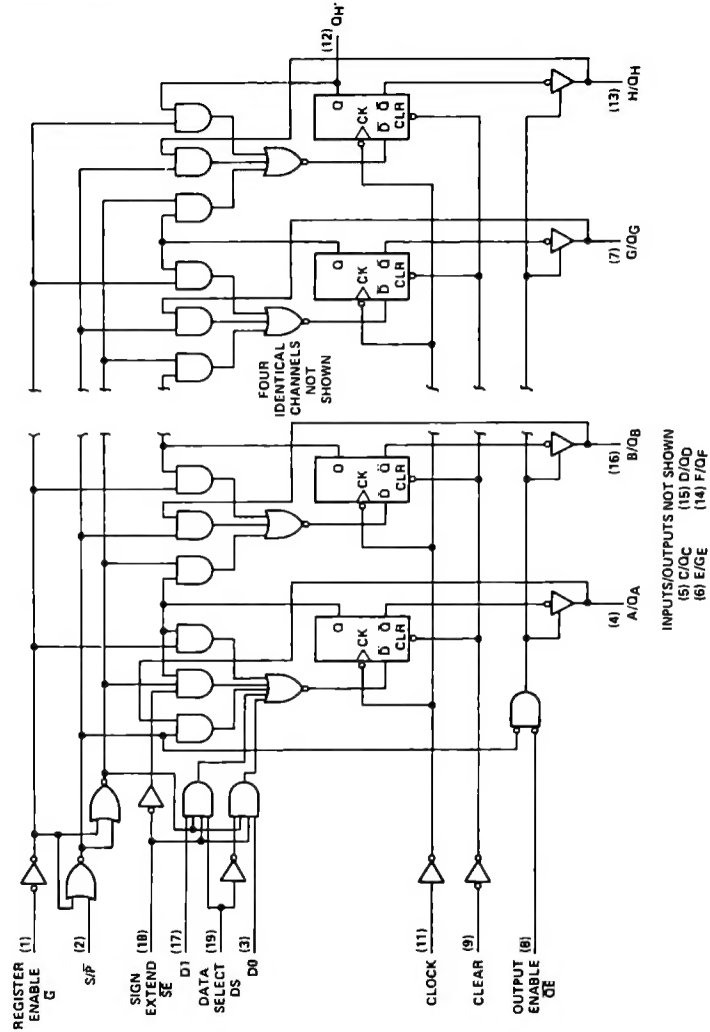
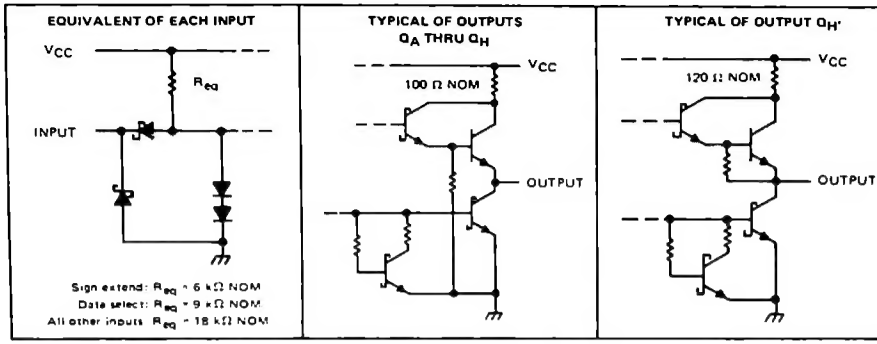
functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54LS322 . . . −55°C to 125°C
SN74LS322 . . . 0°C to 70°C
Storage temperature −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS322			SN74LS322			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−1			−2.6	mA
	Q_H'			−0.4			−0.4	
Low-level output current, I_{OL}	Q_A thru Q_H			12			24	mA
	Q_H'			4			8	
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	14			14			ns
	Clock low	14			14			
Width of clear pulse, $t_{w(clear)}$	Clear low	20			20			ns
Setup time, t_{su}	Data select	10†			10†			ns
	High-level data‡	20†			20†			
	Low-level data‡	20†			20†			
	Clear inactive-state	20†			20†			
Hold time, t_h	Data select	10†			10†			ns
	Data‡	0†			0†			
Operating free-air temperature, T_A		−55		125	0		70	°C

‡Data includes the two serial inputs and the eight input/output data lines.
†The arrow indicates that the rising edge of the clock pulse is used for reference.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS322			SN74LS322			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.2		2.4	3.1		V
		Q_H'	V_{IL} = V_{IL}max,	I_{OH} = MAX	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Q_A thru Q_H	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5	
		Q_H'	V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,			−400			−400	μA
I_I	Input current at maximum input voltage	A thru H	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Data select		V_I = 7 V			0.2			0.2	
		Sign extend		V_I = 7 V			0.3			0.3	
		Any other		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current	A thru H, DS	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Sign extend					60			60	
		Any other					20			20	
I_{IL}	Low-level input current	Data select	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		Sign extend					−1.2			−1.2	
		Any other					−0.4			−0.4	
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX		−30		−130	−30		−130	mA
		Q_H'			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX			35	60		35	60	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	35	50		MHz
t_{PLH}	Clock	Q_H'	C_L = 15 pF, R_L = 2 kΩ, See Note 2		15	25	ns
t_{PHL}					15	25	
t_{PHL}	Clear	Q_H'			20	35	ns
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 665 Ω, See Note 2		15	25	ns
t_{PHL}					15	25	
t_{PHL}	Clear	Q_A thru Q_H			20	35	ns
t_{PZH}	Output enable	Q_A thru Q_H			20	35	ns
t_{PZL}					20	35	
t_{PHZ}	Output enable	Q_A thru Q_H	C_L = 5 pF, R_L = 665 Ω, See Note 2		15	25	ns
t_{PLZ}					15	25	

¶ f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low to high level output
t_{PHL} = propagation delay time, high to low level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

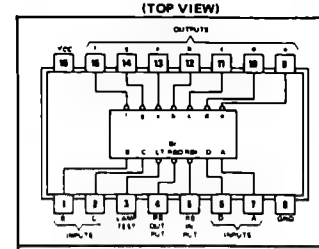
NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 3-11 of *The TTL Data Book For Design Engineers*, Second Edition, LCC4112.

TYPES SN54LS347, SN74LS347
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

BULLETIN NO. DL-S 12596, NOVEMBER 1977

- Low-Voltage Version of SN54LS47/SN74LS47
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Lamp Intensity Modulation Capability

(TOP VIEW)



positive logic: see function tables

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54LS347	low	open-collector	12 mA	7 V	35 mW	J, W
SN74LS347	low	open-collector	24 mA	7 V	35 mW	J, N

SEGMENT IDENTIFICATION

NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.

3. When ripple blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp test input, all segment outputs are on.

† BI/RBO is wire AND logic serving as blanking input (BI) and/or ripple blanking output (RBO).

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54LS347 . . . . . −55°C to 125°C
SN74LS347 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS347			SN74LS347			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			7			7	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			−50			−50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS347			SN74LS347			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −50 μA	2.4	4.2		2.4	4.2		V
V_{OL}	Low level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, $V_{O(off)}$ = 7 V			250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	$I_{O(on)}$ = 12 mA		0.25	0.4		0.25	0.4	V
				$I_{O(on)}$ = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 665 Ω, See Note 4			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112. t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

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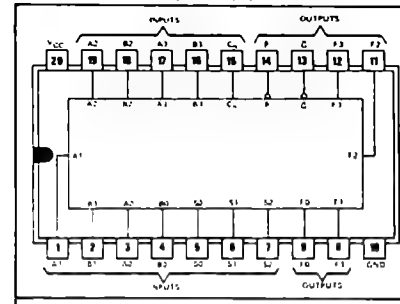
TYPES SN54LS381, SN54LS382, SN74LS381, SN74LS382 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

NOVEMBER 1977

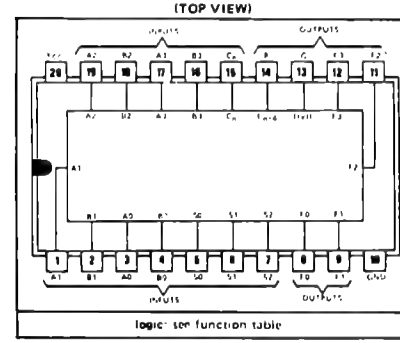
PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C_n	15	CARRY INPUT FOR ADDITION; INVERTED CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
$\overline{P}$ ('LS381 ONLY)	14	INVERTED CARRY PROPAGATE OUTPUT
$\overline{G}$ ('LS381 ONLY)	13	INVERTED CARRY GENERATE OUTPUT
C_{n+4} ('LS382 ONLY)	14	RIPPLE-CARRY OUTPUT
OVR ('LS382 ONLY)	13	OVERFLOW OUTPUT
V_{CC}	20	SUPPLY VOLTAGE
GND	10	GROUND

SN54LS381 . . . J PACKAGE
SN74LS381 . . . J OR N PACKAGE
(TOP VIEW)



SN54LS382 . . . J PACKAGE
SN74LS382 . . . J OR N PACKAGE
(TOP VIEW)



- Fully Parallel 4-Bit ALU's in 20-Pin Package for 0.300-Inch Row Spacing
- Ideally Suited for High-Density Economical Processors
- 'LS381 Features $\overline{G}$ and $\overline{P}$ Outputs for Look-Ahead Carry Cascading
- 'LS382 Features Ripple Carry ($C_n + 4$) and Overflow (OVR) Outputs
- Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:
  - A Minus B
  - B Minus A
  - A Plus B
  - and Five Other Functions

description

The 'LS381 and 'LS382 are low-power Schottky TTL arithmetic logic units (ALUs)/function generators that perform eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. The exclusive-OR, AND, or OR function of the two Boolean variables is provided without the use of external circuitry. Also, the outputs can be cleared (low) or preset (high) as desired. The 'LS381 provides two cascade outputs ($\overline{P}$ and $\overline{G}$) for expansion utilizing SN54S182/SN74S182 look-ahead carry generators. The 'LS382 provides a $C_n + 4$ output to ripple the carry to the C_n input of the next stage. The 'LS382 detects and indicates two's complement overflow condition via the OVR output. The overflow output is logically equivalent to $C_{n+3} \oplus C_{n+4}$. When the 'LS382 is cascaded to handle word lengths longer than four bits in length, only the most significant overflow (OVR) output is used.

The SN54LS381 and SN54LS382 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS381 and SN74LS382 will be characterized for operation from 0°C to 70°C.

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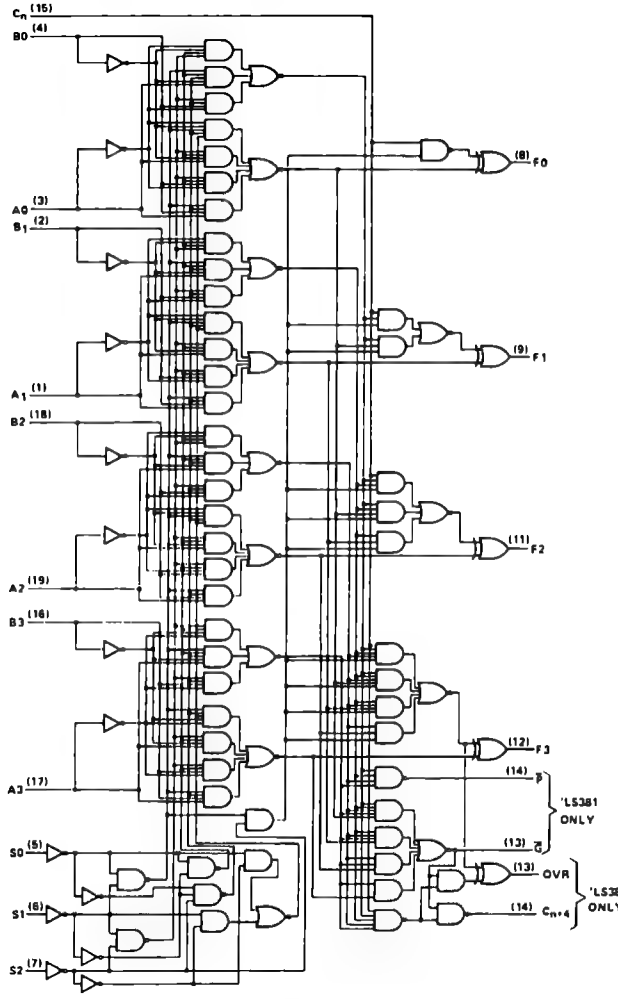
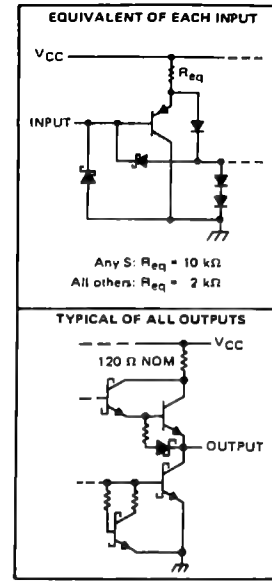
functional block diagram, schematics of inputs and outputs, and function table





FUNCTION TABLE

SELECTION			ARITHMETIC/LOGIC
S2	S1	S0	OPERATION
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A + B
H	L	H	A ⊕ B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

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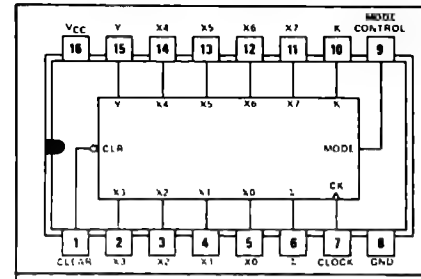
TO BE ANNOUNCED

TYPES SN54LS384, SN74LS384
8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

NOVEMBER 1977

- Two's-Complement Multiplication
- Magnitude Only Multiplication
- Cascadable for Any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- Serial Multiplier Data Input
- Serial Data Output for Multiplication Product
- 40 MHz Typical Maximum Clock Frequency

SN54LS384 . . . J OR W PACKAGE
SN74LS384 . . . J OR N PACKAGE
(TOP VIEW)



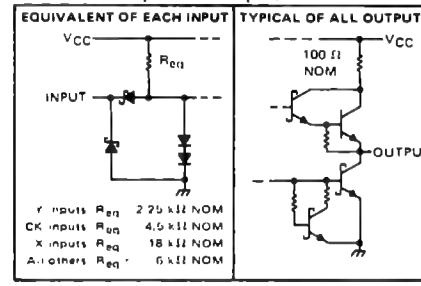
positive logic: see function table

description

The 'LS384 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's-complement form to produce a two's-complement product without external correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. These X latches are controlled via the clear input. When the clear input is low, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is high, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream, least significant bit first. The product is clocked out the Σ output, least significant bit first.

schematics of inputs and outputs



The multiplication of an m-bit multiplicand by an n-bit multiplier results in an (m + n)-bit product. The 'LS384 must be clocked for m + n clock cycles to produce this two's complement product. The n-bit multiplier (Y-input) sign bit data must be extended for the remaining m bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The Σ output of one device is connected to the K input of the succeeding device when cascading. The mode input is used to indicate which device contains the most significant bit. The mode input is wired high or low depending on the position of the 8-bit slice in the total X word length. The device with the most significant bit is wired low and all lower order bit packages are wired high.

The SN54LS384 will be characterized for operation over the full military temperature range from −55°C to 125°C. The SN74LS384 will be characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				INTERNAL	OUTPUT	FUNCTION
CLR	CK	X_i	Y	Y_{-1}	Σ	
L	X	Data	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	↓	X	L	L	Output	Shift sum register
H	↑	X	L	H	per	Add multiplicand to sum register and shift
H	↓	X	H	L	Booth's	Subtract multiplicand from sum register and shift
H	↑	X	H	H	algorithm	Shift sum register

H = high-level, L = low level, X = irrelevant, ↑ = low to high level transition, ↓ = high to low level transition

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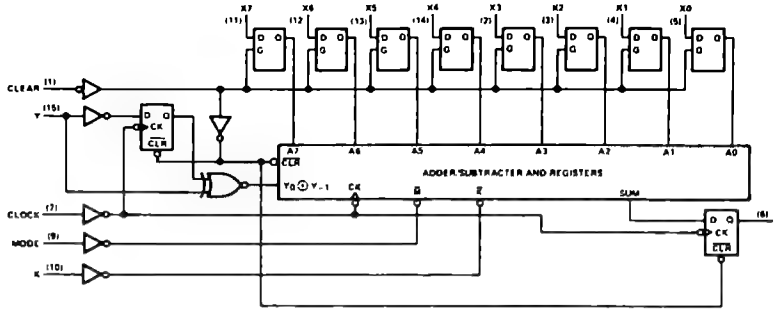
functional block diagram



TYPICAL APPLICATION DATA

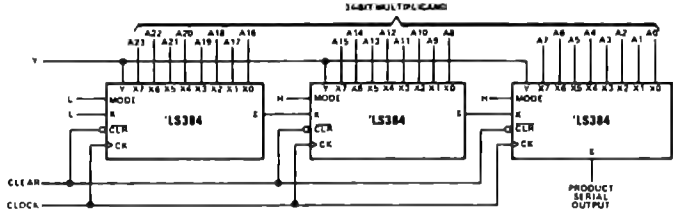


FIGURE 1–BASIC 24-BIT SERIAL/PARALLEL CONNECTION

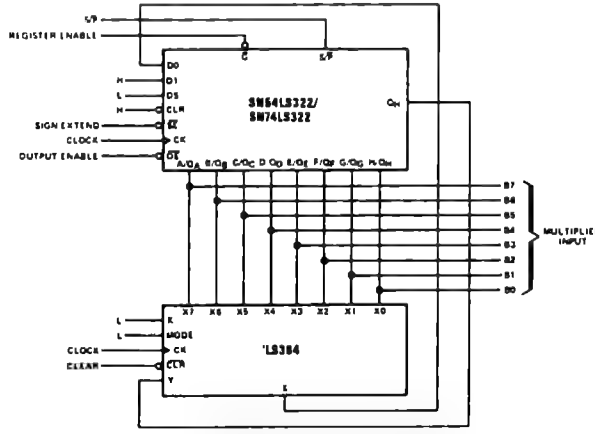


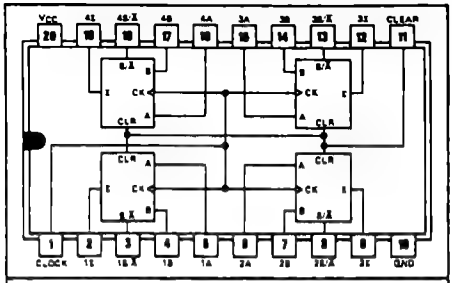
FIGURE 2–8-BIT BY 8-BIT MULTIPLIER, BUS ORGANIZED, WITH 8-BIT TRUNCATED PRODUCT

TYPES SN54LS385, SN74LS385
QUADRUPLE SERIAL ADDERS/SUBTRACTORS

BULLETIN NO. DL-S 12599, NOVEMBER 1977

- Four Synchronous Elements in a Single 20-Pin Package
- Buffered Clock and Direct Clear Inputs
- Independent Two's-Complement Addition/Subtraction

SN54LS385 . . . . J PACKAGE
SN74LS385 . . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

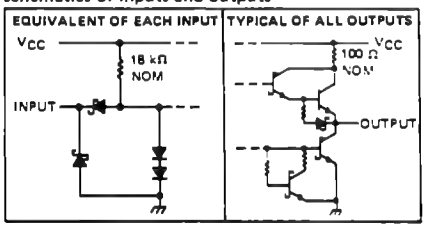
description

The 'LS385 is a general purpose adder/subtractor and is particularly useful as a companion part to the SN54LS384/SN74LS384 serial/parallel two's-complement multiplier. The 'LS385 contains four independent adder/subtractor elements with common clock and clear.

Each of the four independent sum (Σ) outputs reflects its respective A and B input as controlled by the S/$\overline{A}$ control. When S/$\overline{A}$ is high the Σ function is A minus B. When S/$\overline{A}$ is low the Σ function is A plus B.

When low, the clear input asynchronously resets the sum flip-flop low and the carry flip-flop either high in the subtract mode or low in the add mode. The clock is positive-edge triggered and controls the sum and carry flip-flops according to the function table.

schematics of inputs and outputs

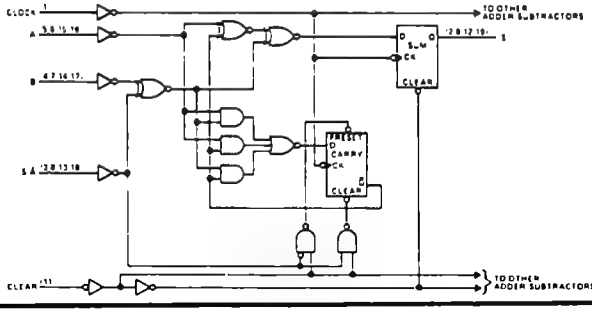


FUNCTION TABLE

SELECTED FUNCTION	INPUTS CLEAR	S/A	A	B	CLOCK	INTERNAL CARRY D INPUT BEFORE ↑	INTERNAL CARRY D INPUT AFTER ↑	Σ OUTPUT AFTER ↑
Clear	L	L	X	X	X	L	L	L
	L	H	X	X	X	H	H	L
Add	H	L	L	L	↑	L	L	L
	H	L	L	L	↑	H	L	H
	H	L	L	H	↑	L	L	H
	H	L	L	H	↑	H	H	L
	H	L	H	L	↑	L	L	H
	H	L	H	L	↑	H	H	L
	H	L	H	H	↑	L	H	L
	H	L	H	H	↑	H	H	H
Subtract	H	H	L	L	↑	L	L	H
	H	H	L	L	↑	H	H	L
	H	H	L	H	↑	L	L	L
	H	H	L	H	↑	H	L	H
	H	H	H	L	↑	L	H	L
	H	H	H	L	↑	H	H	H
	H	H	H	H	↑	L	L	H
	H	H	H	H	↑	H	H	L

H = high level, L = low level, X = irrelevant,
↑ = transition from low to high level at the clock input

functional block diagram (each adder/subtractor)



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recommended operating conditions

	SN54LS385			SN74LS385			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	16			16			ns
Setup time, t_{su}	10			10			ns
Hold time, t_h	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS385			SN74LS385			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			48	75		48	75	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Note 3	30	40		MHz
t_{PLH}	Clock	Σ			14	22	ns
t_{PHL}					18	27	
t_{PHL}	Clear	Σ			18	30	ns

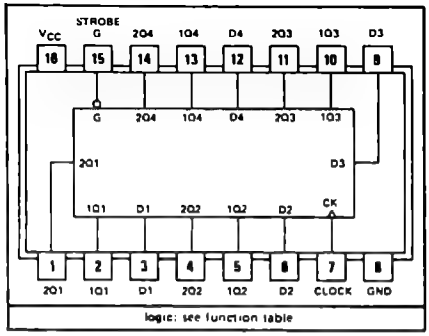
◇ f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112

TYPES SN54LS396, SN74LS396
OCTAL STORAGE REGISTERS

BULLETIN NO. DL-S 12502, MARCH 1977

- Parallel Access
- Typical Propagation Delay Time . . . 20 ns
- Typical Power Dissipation . . . 120 mW
- Applications:
  N-Bit Storage Files
  Hex/BCD Serial-To-Parallel Converters

SN54LS396 . . . J OR W PACKAGE
SN74LS396 . . . J OR N PACKAGE
(TOP VIEW)



description

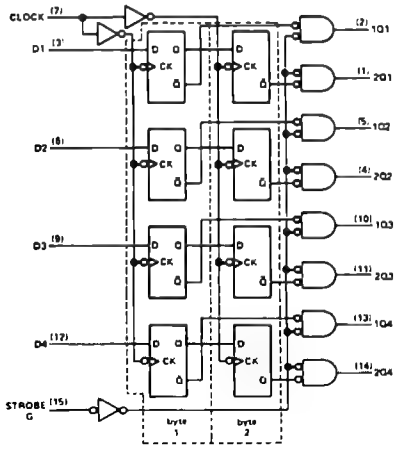
These octal registers are organized as two 4-bit bytes of storage. Upon application of a positive-going clock signal, the information stored in byte 1 is transferred into byte 2 as a new 4-bit byte is loaded into the byte 1 location via the four data lines. The full 8-bit word is available at the outputs after two clock cycles. Both the clock and the strobe lines are fully buffered.

FUNCTION TABLE

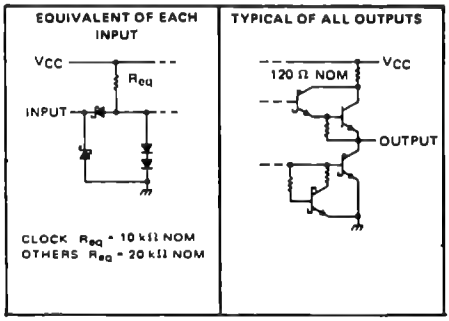
INPUTS						OUTPUTS							
STROBE G	CLOCK	DATA D1	DATA D2	DATA D3	DATA D4	1Q1	1Q2	1Q3	1Q4	2Q1	2Q2	2Q3	2Q4
H	X	X	X	X	X	L	L	L	L	L	L	L	L
L	↑	a	b	c	d	a	b	c	d	$1Q1_n$	$1Q2_n$	$1Q3_n$	$1Q4_n$

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↑ = transition from low to high level
$1Q1_n$, $1Q2_n$, $1Q3_n$, $1Q4_n$ = the level of 1Q1, 1Q2, 1Q3, and 1Q4, respectively, before the most recent ↑ transition of the clock

functional block diagram



schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS396 . . . . . −55°C to 125°C
SN74LS396 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54LS396			SN74LS396			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS396			SN74LS396			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Clock input	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
		Other inputs					0.1			0.1	
I_{IH}	High-level input current	Clock input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Other inputs					20			20	
I_{IL}	Low-level input current	Clock input	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		Other inputs					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		24	40		24	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 2 kΩ, See Note 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from strobe			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from strobe			20	30	

NOTE 3: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

TO BE ANNOUNCED

TYPE SN54LS442, SN54LS443, SN54LS444, SN74LS442, SN74LS443, SN74LS444 QUADRUPLE TRI-DIRECTIONAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

NOVEMBER 1977

- 3-Way Asynchronous Communication
- P-N-P Inputs Reduce DC Loading
- On-Chip Bus Selection Decoding
- Input Hysteresis Improves Noise Margin
- 3-State Outputs Rated at 12/24 mA I_{OL} and −12/−15 mA I_{OH} for SN54LS'/SN74LS', Respectively

description

These bus transceivers are designed for asynchronous three-way communication between four-line data buses. They give the designer a choice of selecting inverting, noninverting, or a combination of inverting and noninverting outputs. The devices feature high fan-out, improved fan-in, and 400-mV noise margin.

The S0 and S1 inputs select the bus from which data are to be transferred. The $\overline{G}$ inputs enable the bus or buses to which data are to be transferred. The port for any bus selected for input and any other bus not enabled for output will be at high impedance.

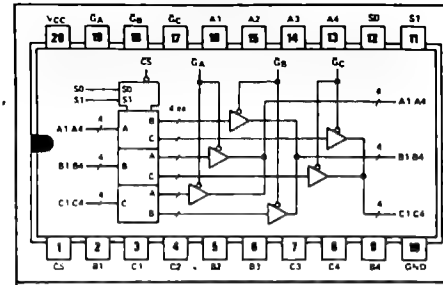
The SN54LS442, SN54LS443, and SN54LS444 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS442, SN74LS443, and SN74LS444 will be characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						TRANSFERS BETWEEN BUSES		
$\overline{CS}$	S1	S0	$\overline{G}_A$	$\overline{G}_B$	$\overline{G}_C$	'LS442	'LS443	'LS444
H	X	X	X	X	X	None	None	None
X	H	H	X	X	X	None	None	None
X	X	X	H	H	H	None	None	None
X	L	L	X	H	H	None	None	None
X	L	H	H	X	H	None	None	None
X	H	L	H	H	X	None	None	None
L	L	L	X	L	L	A • B, A • C	$\overline{A}$ • B, $\overline{A}$ • C	$\overline{A}$ • B, $\overline{A}$ • C
L	L	H	L	X	L	B • C, B • A	$\overline{B}$ • C, $\overline{B}$ • A	B • C, $\overline{B}$ • A
L	H	L	L	L	X	C • A, C • B	$\overline{C}$ • A, $\overline{C}$ • B	$\overline{C}$ • A, C • B
L	L	L	X	L	H	A • B	$\overline{A}$ • B	$\overline{A}$ • B
L	L	H	H	X	L	B • C	$\overline{B}$ • C	B • C
L	H	L	L	H	X	C • A	$\overline{C}$ • A	$\overline{C}$ • A
L	L	L	X	H	L	A • C	$\overline{A}$ • C	$\overline{A}$ • C
L	L	H	L	X	H	B • A	$\overline{B}$ • A	$\overline{B}$ • A
L	H	L	H	L	X	C • B	$\overline{C}$ • B	C • B

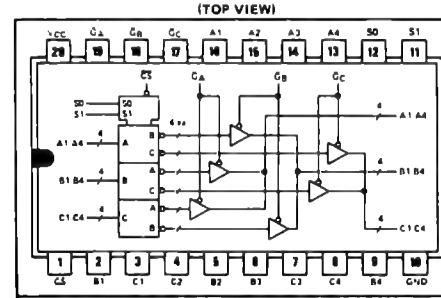
H = high level, L = low level, X = irrelevant,
A • B = noninverting transfer from A to B,
$\overline{B}$ • C = inverting transfer from B to C,
I/O ports to which data are not transferred are at high impedance

SN54LS442 . . . J PACKAGE
SN74LS442 . . . J OR N PACKAGE
(TOP VIEW)



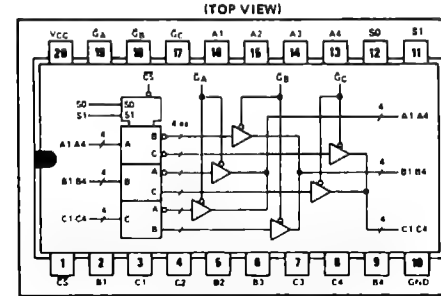
positive logic: see function table

SN54LS443 . . . J PACKAGE
SN74LS443 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS444 . . . J PACKAGE
SN74LS444 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

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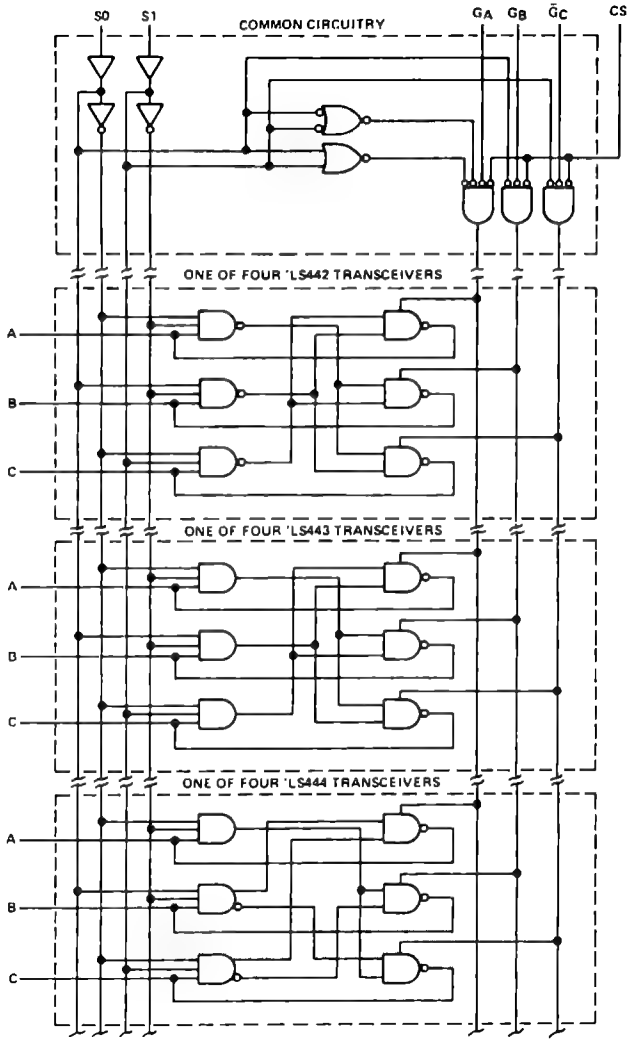
functional block diagram (composite showing one of four transceivers from each type)



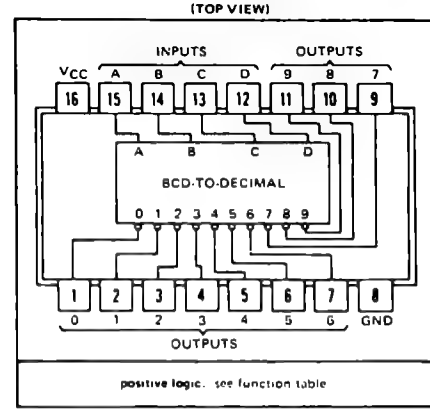
TYPES SN54LS445, SN74LS445
BCD-TO-DECIMAL DECODERS/DRIVERS

BULLETIN NO. DL-S 12598, NOVEMBER 1977

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Low-Voltage Version of SN54LS145/ SN74LS145
- Full Decoding of Input Logic
- SN74LS445 Has 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation . . . 35 mW Typical

SN54LS445 . . . J OR W PACKAGE
SN74LS445 . . . J OR N PACKAGE
(TOP VIEW)



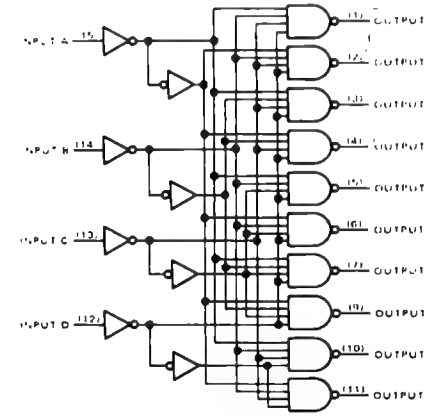
logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

functional block diagram



description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high performance, n-p-n output transistors designed for use as indicator/ relay drivers or as open-collector logic-circuit drivers. Each of the output transistors will sink up to 80 milliamperes of current. Each input is one Series 54LS/ 74LS standard load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 35 milliwatts.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS445 . . . . . −55°C to 125°C
SN74LS445 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS445			SN74LS445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			7			7	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS445			SN74LS445			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					7			7	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
$I_{O(off)}$	Off-state output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 7 V			250			250	µA
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{IL} = V_{IL} max	I_{OL} = 80 mA					2.0	3	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		7	13		7	13	mA

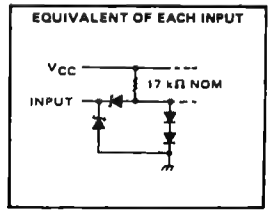
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

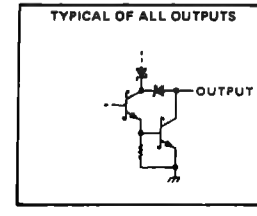
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 665 Ω, See Note 4		50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			50	ns

NOTE 4: Load circuit and waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition, LCC 4112.

schematic of inputs and outputs



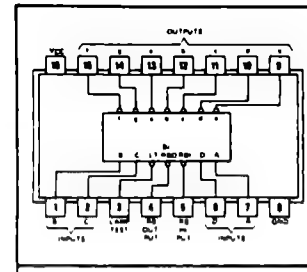


TYPES SN54LS447, SN74LS447
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

BULLETIN NO. DL-S 12697, NOVEMBER 1977

- Low-Voltage Version of SN54LS247/SN74LS247
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Lamp Intensity Modulation Capability

(TOP VIEW)



positive logic: see function tables

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54LS247	low	open-collector	12 mA	7 V	35 mW	J, W
SN74LS247	low	open-collector	24 mA	7 V	35 mW	J, N

NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

SEGMENT IDENTIFICATION

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54LS447 . . . . . −55°C to 125°C
SN74LS447 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

		SN54LS447			SN74LS447			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			7			7	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			−50			−50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS447			SN74LS447			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −50 μA	2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, $V_{O(off)}$ = 7 V			250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	$I_{O(on)}$ = 12 mA		0.25	0.4		0.25	0.4	V
				$I_{O(on)}$ = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 665 Ω, See Note 4			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112. t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

TO BE ANNOUNCED

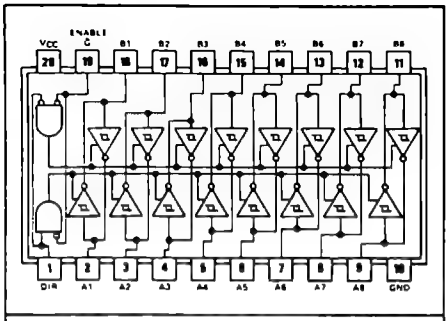
TYPES SN54LS640, SN54LS641, SN54LS642, SN54LS645 SN74LS640, SN74LS641, SN74LS642, SN74LS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

NOVEMBER 1977

- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- P-N-P Inputs Reduce D-C Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

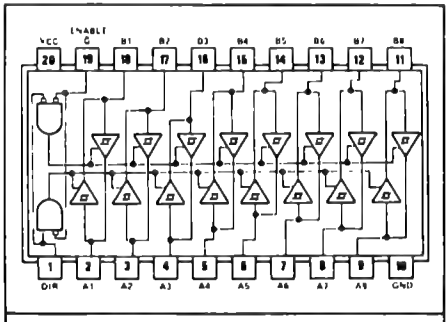
TYPE	LOGIC	OUTPUT
'LS640	Inverting	3-State
'LS641	True	Open-Collector
'LS642	Inverting	Open-Collector
'LS645	True	3-State

SN54LS640, SN54LS642 . . . J PACKAGE
SN74LS640, SN74LS642 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS641, SN54LS645 . . . J PACKAGE
SN74LS641, SN74LS645 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

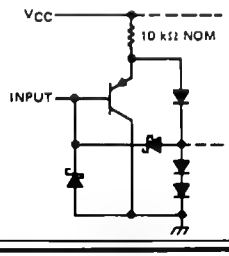
FUNCTION TABLE

ENABLE G	DIRECTION CONTROL DIR	OPERATION 'LS640, 'LS642	OPERATION 'LS641, 'LS645
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

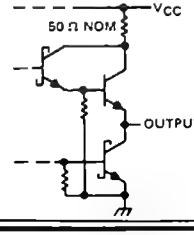
H = high level, L = low level, X = irrelevant

schematics of inputs and outputs

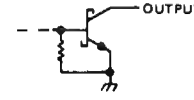
EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS OF 'LS640, 'LS645



TYPICAL OF OUTPUTS OF 'LS641, 'LS642



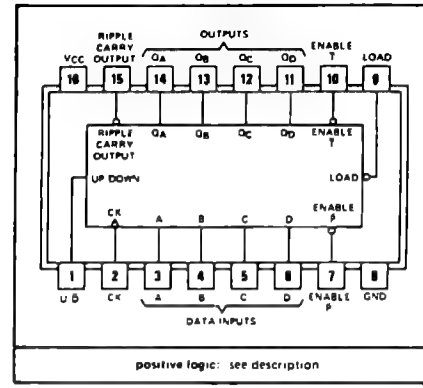
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES SN54LS668, SN54LS669, SN74LS668, SN74LS669
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

BULLETIN NO. DL-S 12517, APRIL 1977 - REVISED NOVEMBER 1977

'LS668 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS669 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

SERIES SN54LS' . . . J OR W PACKAGE
SERIES SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

Programmable Look-Ahead Up/Down Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit
- Buffered Outputs

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS668, 'LS669	35 MHz	35 MHz	100 mW

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS668 are decade counters and the 'LS669 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable, that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

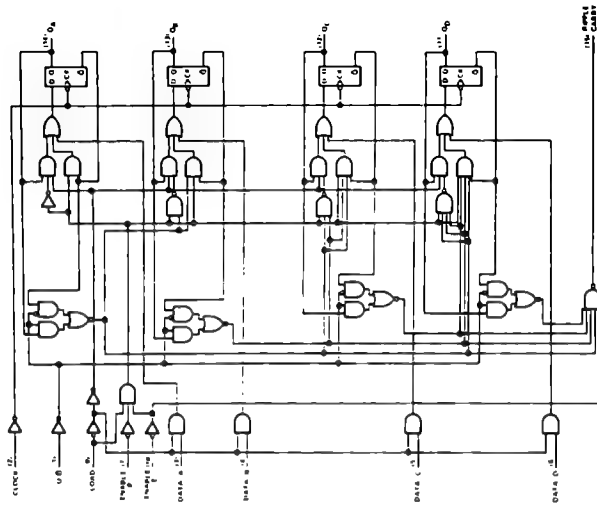
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

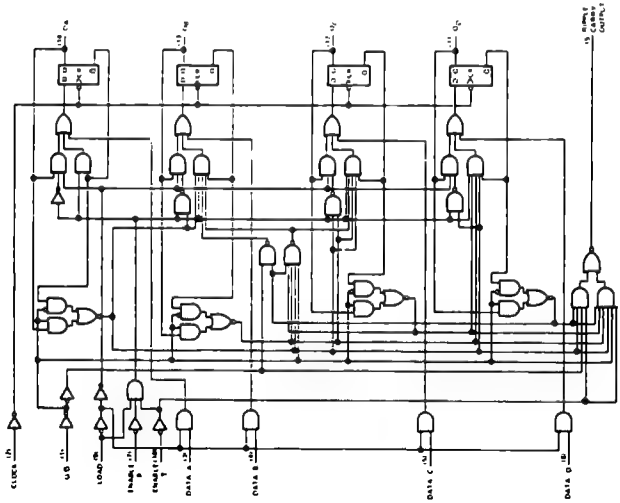
The 'LS668 and 'LS669 are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time, reduced input currents I_{IH} and I_{IL}, and all buffered outputs.

functional block diagrams

SN54LS669, SN74LS669, BINARY COUNTERS



SN54LS668, SN74LS668, DECADE COUNTERS



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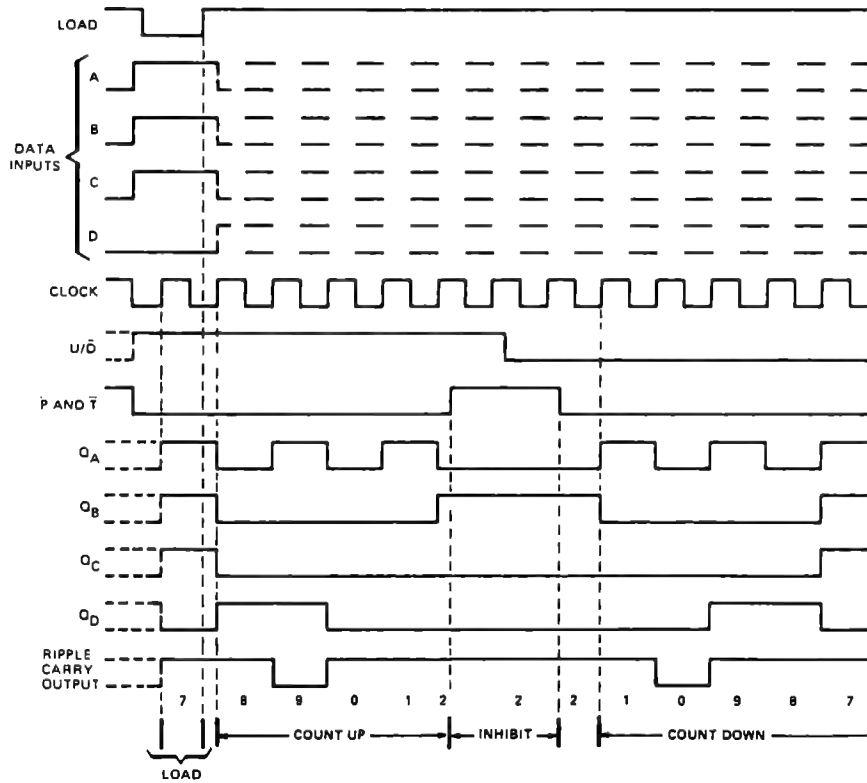
'LS668 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

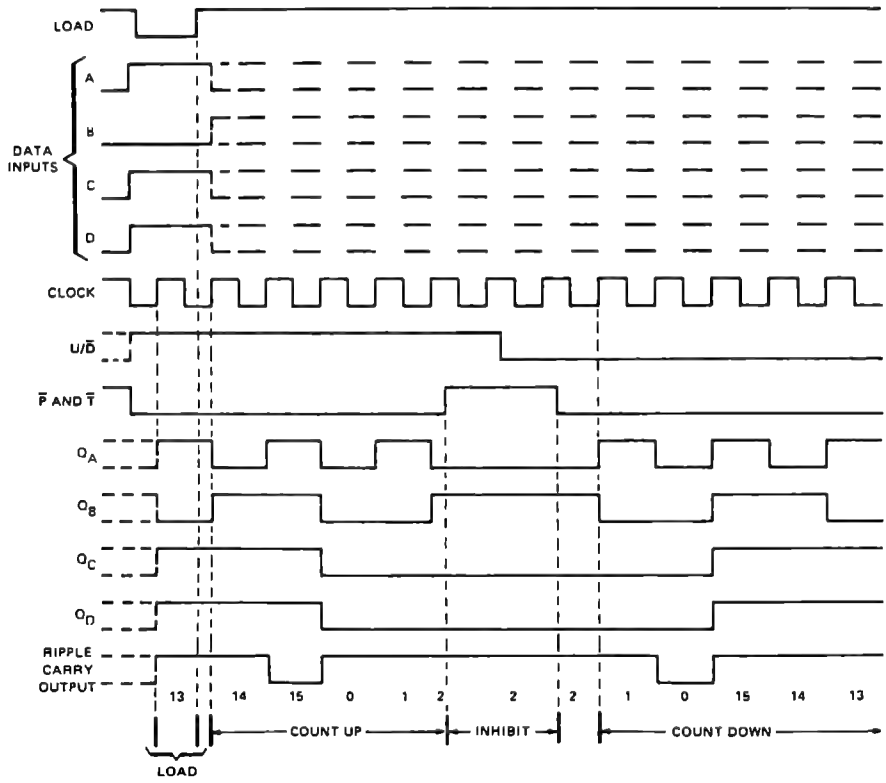


'LS669 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



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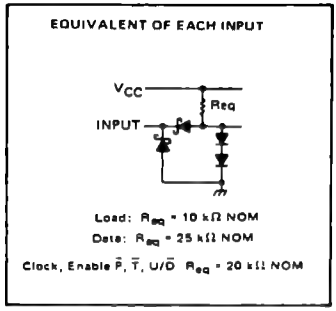
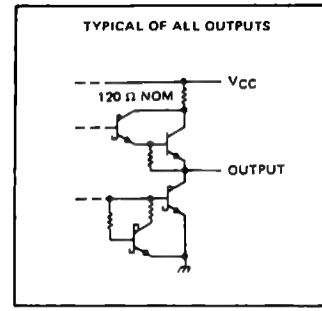
schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS668, SN54LS669 . . . −55°C to 125°C
SN74LS668, SN74LS669 . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

		SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1)		25			25			ns
Setup time, t_{su} (see Figure 1)	Data inputs A, B, C, D	20			20			ns
	Enable P̄ or T̄	20			20			
	Load	25			25			
	Up/Down	30			30			
Hold time at any input with respect to clock, t_h (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		Clock, $\overline{T}$					0.1			0.1	
		Load					0.2			0.2	
I_{IH}	High-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Clock, $\overline{T}$					20			20	
		Load					40			40	
I_{IL}	Low-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Clock, $\overline{T}$					−0.4			−0.4	
		Load					−0.8			−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		20	34		20	34	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 2 and 3	25	32		MHz
t_{PLH}	Clock	Ripple carry			26	40	ns
t_{PHL}					40	60	
t_{PLH}	Clock	Any Q			18	27	ns
t_{PHL}					18	27	
t_{PLH}	Enable $\overline{T}$	Ripple carry			11	17	ns
t_{PHL}					29	45	
t_{PLH}◇	Up/Down	Ripple carry			22	35	ns
t_{PHL}◇					26	40	

¶f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.
◇Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668 or 15 for 'LS669), the ripple carry output will be out of phase.

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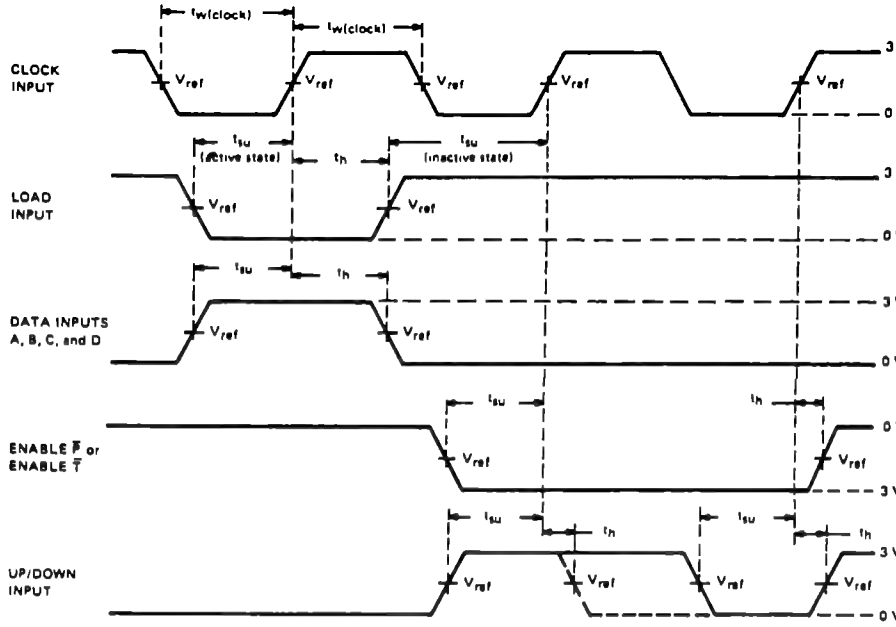
PARAMETER MEASUREMENT INFORMATION

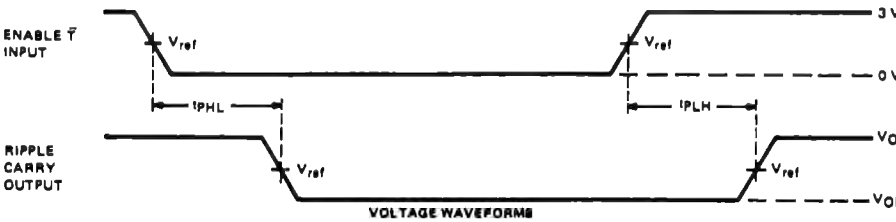


VOLTAGE WAVEFORMS

NOTES A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω, t_r ≤ 15 ns, t_f ≤ 6 ns.

B. V_{ref} = 1.3 V.

FIGURE 1–PULSE WIDTHS, SETUP TIMES, HOLD TIMES



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω; t_r ≤ 15 ns, t_f ≤ 6 ns.

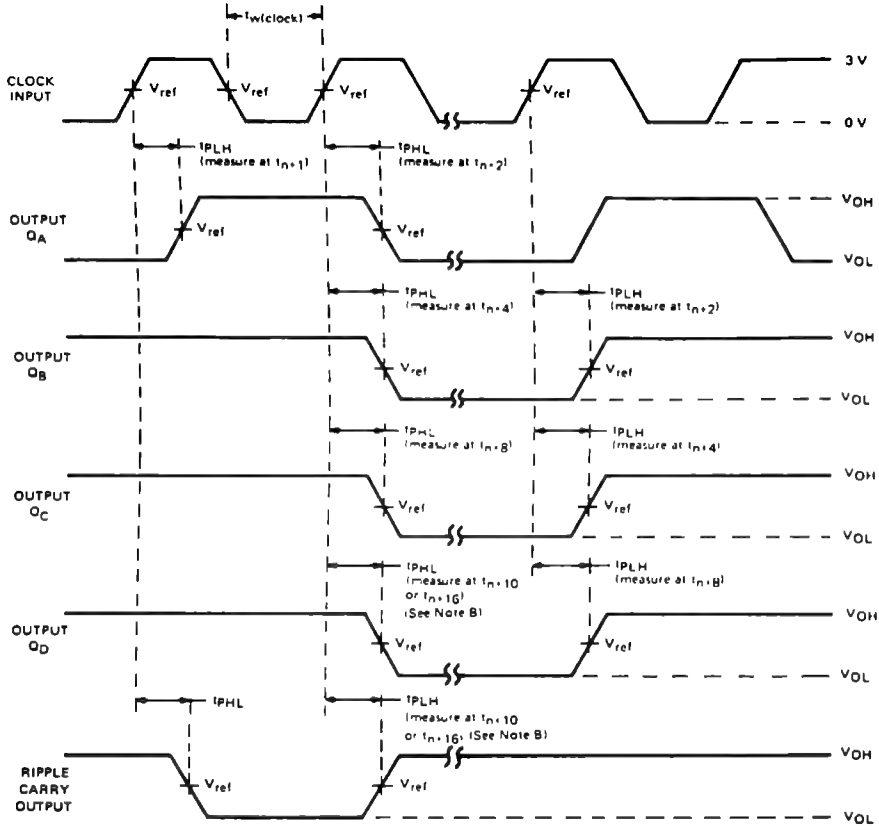
B. t_{PLH} and t_{PHL} from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'LS668, all Q outputs high for 'LS669).

C. V_{ref} = 1.3 V.

D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668, or 15 for 'LS669) the ripple carry output will be out of phase.

FIGURE 2–PROPAGATION DELAY TIMES TO CARRY OUTPUT

PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

NOTES A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the 'LS668 and at t_{n+16} for the 'LS669, where t_n is the bit time when all outputs are low.

C. $V_{ref} = 1.3$ V.

FIGURE 3–PROPAGATION DELAY TIMES FROM CLOCK

TEXAS INSTRUMENTS
INCORPORATED
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TYPES SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

NOVEMBER 1977

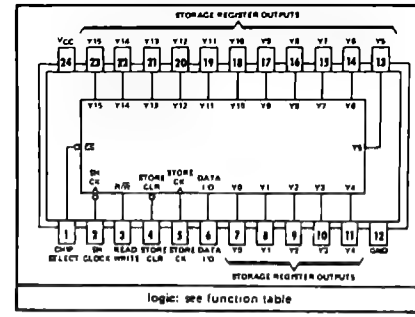
'LS673

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

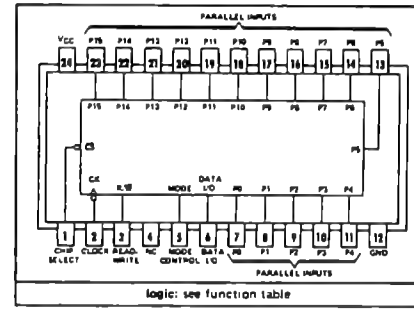
'LS674

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

SN54LS673 . . . J OR W PACKAGE
SN74LS673 . . . J OR N PACKAGE
(TOP VIEW)



SN54LS674 . . . J OR W PACKAGE
SN74LS674 . . . J OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (I/O) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip select ($\overline{CS}$) input disables both the shift-register clock and the storage-register clock and places the data I/O in the high-impedance state. The storage-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip select, input. The shift clock should be low during the low-to-high transition of chip select and the storage clock should be low during the high-to-low transition of chip select.

SN54LS674, SN74LS674

The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (I/O) port provides access for entering serial data or reading the shift-register word in a recirculating loop.

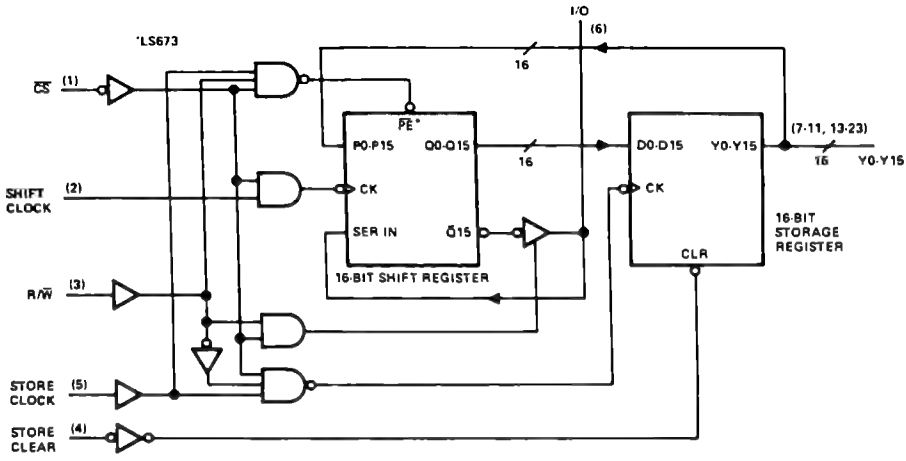
The device has four basic modes of operation:

1) Hold (do nothing)
2) Write (serially via input/output)
3) Read (serially)
4) Load (parallel via data inputs)

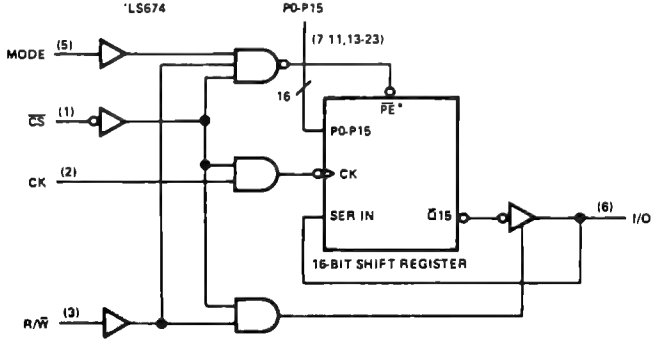
Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

functional block diagrams

SN54LS673, SN74LS673



SN54LS674, SN74LS674



*When $\overline{PE}$ is low, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place.

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'LS673 FUNCTION TABLE

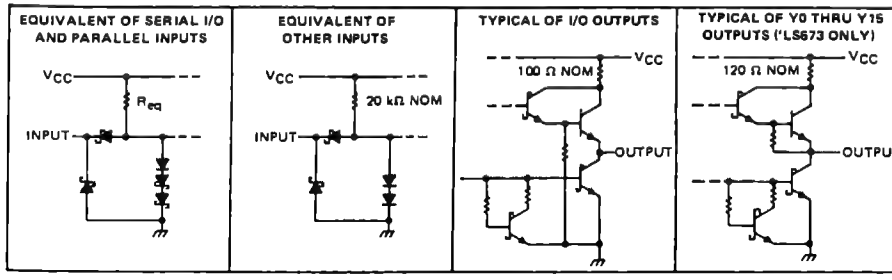
INPUTS					SERIAL	
CHIP SELECT	SHIFT REG R/$\overline{W}$	SHIFT REG CLOCK	STORAGE CLEAR	STORAGE CLOCK	I/O PORT	OPERATION
X	L	X	L	X	Z	L input to ST CLR clears
H	X	X	L	X	Z	Storage registers; I/O depends
L	H	X	L	X	Q15	on $\overline{CS}$ and R/$\overline{W}$.
H	X	X	X	X	Z	No shifting or loading
L	L	↑	X	X	Z	Shift and write (load)
L	H	↓	X	L	Q14n	Shift and read
L	H	↑	L	H	L	Reload shift register from
L	H	↓	H	H	Y15n	storage, no shifting
L	L	X	H	↑	Z	Load storage from shift register

'LS674 FUNCTION TABLE

INPUTS				I/O	OPERATION
$\overline{CS}$	R/$\overline{W}$	MODE	CLOCK	PORT	
H	X	X	X	Z	Do nothing
L	L	X	↑	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↑	P15	Parallel load

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input including transitions)
Z = high impedance, I/O in input mode
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock
Q15 = present content of 15th bit of the shift register
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.
P15 = level of input P15

schematics of inputs and outputs

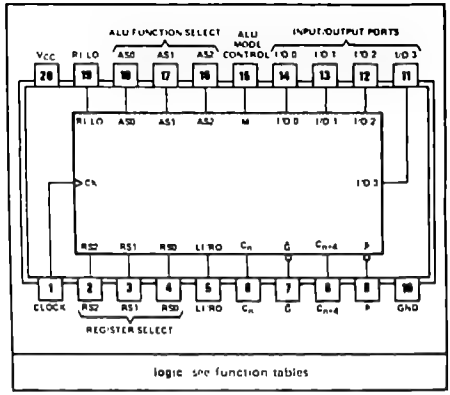


TYPES SN54LS681, SN74LS681
4-BIT PARALLEL BINARY ACCUMULATORS

NOVEMBER 1977

- Full 4-Bit Binary Accumulator in a Single 20-Pin Package
- Contains Two Synchronous Registers:
  Word A
  Word B Shift/Accumulator
- 16 Arithmetic Operations Including B Minus A and A Minus B
- 16 Logic-Mode Operations
- Expandable to Handle N-Bit Words with Full Carry Look-Ahead
- Bus Driving I/O Ports

SN54LS681 . . . J PACKAGE
SN74LS681 . . . J OR N PACKAGE
(TOP VIEW)



description

These low-power Schottky IC's integrate a high-speed arithmetic logic unit (ALU) complete with word A and word B registers on a single chip. The ALU performs 16 arithmetic and 16 logic functions (see Tables 1 and 2). Full carry look-ahead is provided for fast carry of four-bit words. The carry input (C_n) and propagate and generate outputs ($\overline{P}$ and $\overline{G}$) are provided for direct use with SN54S182/SN74S182 carry look-ahead generators for optimum performance with longer words.

The A and B registers are controlled by three inputs (RS0, RS1, and RS2). These pins define eight distinct register modes (see Table 3). The A register is a simple storage register while the B register is a combination storage/shift/accumulator register. The contents of the A and B registers provide the A and B words for the ALU.

Four I/O ports (I/O 0 thru I/O 3) are provided for parallel loading of word A and/or word B into their respective registers. These same ports also serve as bus driving outputs for the ALU/accumulator results (F_j). Two additional I/O ports (RI/LO and LI/RO) are provided to allow expansion of the accumulator for words greater than four bits in length.

The A or B register can be parallel loaded from the four I/O ports. The B register can also be parallel loaded from the ALU as an accumulator register and in addition, the B register can be serially loaded from either the RI/LO or the LI/RO ports.

The SN54LS681 will be characterized for operation over the full military temperature range from −55°C to 125°C. The SN74LS681 will be characterized for operation from 0°C to 70°C.

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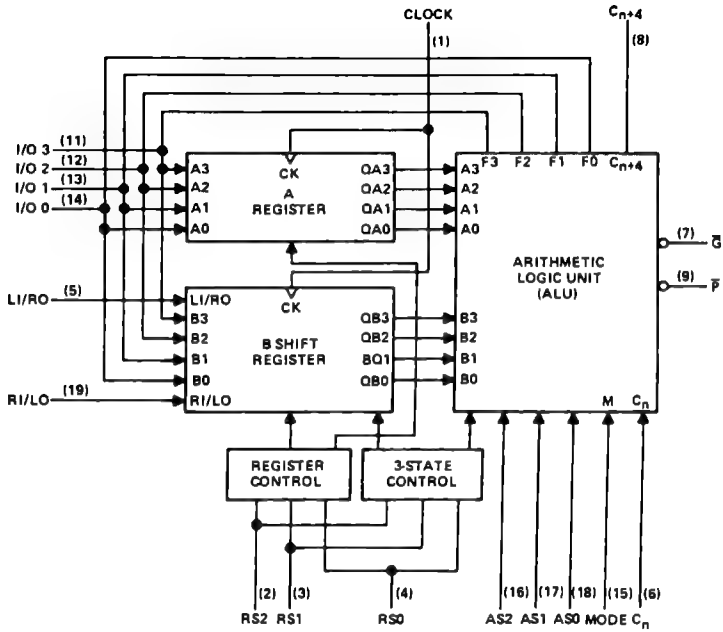
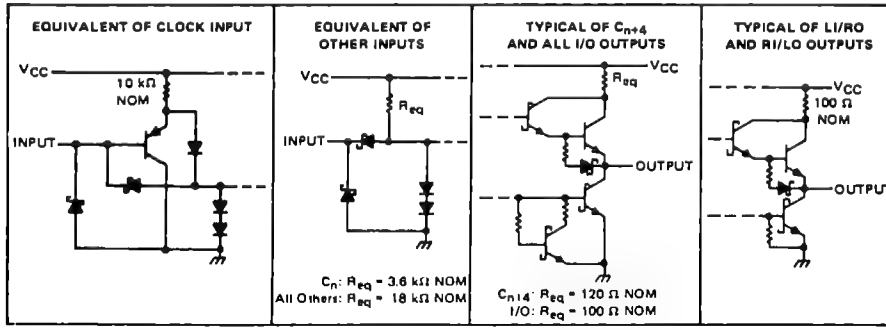
functional block diagram



schematics of inputs and outputs



FUNCTION TABLES

TABLE 1 – ARITHMETIC FUNCTIONS

Mode Control (M) = Low

ALU SELECTION			ACTIVE-HIGH DATA	
			C_n = H	C_n = L
AS2	AS1	AS0	(with carry)	(no carry)
L	L	L	$F_j = L$	$F_j = H$
L	L	H	F = B MINUS A	F = B MINUS A MINUS 1
L	H	L	F = A MINUS B	F = A MINUS B MINUS 1
L	H	H	F = A PLUS B PLUS 1	F = A PLUS B
H	L	L	F = B PLUS 1	$F_j = B_j$
H	L	H	$F = \overline{B}$ PLUS 1	$F_j = \overline{B}_j$
H	H	L	F = A PLUS 1	$F_j = A_j$
H	H	H	$F = \overline{A}$ PLUS 1	$F_j = \overline{A}_j$

TABLE 2 – LOGIC FUNCTIONS

Mode Control (M) = High

ALU SELECTION			ACTIVE-HIGH DATA	
			C_n = H	C_n = L
AS2	AS1	AS0	(with carry)	(no carry)
L	L	L	$F_0 = H$, $F_1 = F_2 = F_3 = L$	$F_j = L$
L	L	H	$F_j = A_j \oplus B_j$ PLUS 1	$F_j = A_j \oplus B_j$
L	H	L	$F_j = \overline{A_j \oplus B_j}$ PLUS 1	$F_j = \overline{A_j \oplus B_j}$
L	H	H	$F_j = L$	$F_j = H$
H	L	L	$F_j = A_j B_j$ PLUS 1	$F_j = A_j B_j$
H	L	H	$F_j = \overline{A_j + B_j}$ PLUS 1	$F_j = \overline{A_j + B_j}$
H	H	L	$F_j = \overline{A_j B_j}$ PLUS 1	$F_j = \overline{A_j B_j}$
H	H	H	$F_j = A_j + B_j$ PLUS 1	$F_j = A_j + B_j$

TABLE 3 – REGISTER FUNCTIONS

FUNCTION	INPUTS BEFORE L TO H CLOCK TRANSITION									INTERNAL OUTPUTS AFTER L TO H CLOCK TRANSITION												
	REGISTER SELECTION			DATA INPUTS						A REGISTER				B SHIFT REGISTER						ALU			
	RS2	RS1	RS0	LI/RO	I/O 3	I/O 2	I/O 1	I/O 0	RI/LO	QA3	QA2	QA1	QA0	LI/RO	QB3	QB2	QB1	QB0	RI/LO	F3	F2	F1	F0
ACCUM	L	L	L	Z	F3	F2	F1	F0	Z	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	Z	$F3_n$	$F2_n$	$F1_n$	$F0_n$	Z	F3	F2	F1	F0
LOAD B	L	L	H	Z	b3	b2	b1	b0	Z	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	Z	b3	b2	b1	b0	Z	Z	Z	Z	Z
LEFT SHIFT LOGICAL	L	H	L	ll	F3	F2	F1	F0	QB0	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	ll	ll	$QB3_n$	$QB2_n$	$QB1_n$	$QB1_n$	F3	F2	F1	F0
LEFT SHIFT ARITH	L	H	H	ll	F3	F2	F1	F0	QB0	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	ll	$QB3_n$	ll	$QB2_n$	$QB1_n$	$QB1_n$	F3	F2	F1	F0
RIGHT SHIFT LOGICAL	H	L	L	QB3	F3	F2	F1	F0	rl	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	$QB2_n$	$QB2_n$	$QB1_n$	$QB0_n$	rl	rl	F3	F2	F1	F0
RIGHT SHIFT ARITH	H	L	H	QB2	F3	F2	F1	F0	rl	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	$QB1_n$	$QB3_n$	$QB1_n$	$QB0_n$	rl	rl	F3	F2	F1	F0
HOLD	H	H	L	Z	F3	F2	F1	F0	Z	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	Z	$QB3_0$	$QB2_0$	$QB1_0$	$QB0_0$	Z	$F3_0$	$F2_0$	$F1_0$	$F0_0$
LOAD A	H	H	H	Z	a3	a2	a1	a0	Z	a3	a2	a1	a0	Z	$QB3_0$	$QB2_0$	$QB1_0$	$QB0_0$	Z	Z	Z	Z	Z

H = high level (steady state)
L = low level (steady state)
Z = high impedance (output off)
a0 . . . a3, b0 . . . b3 = the level of steady-state condition at I/O 0 thru I/O 3, respectively and intended as A or B input data
F0 . . . F3 = Internal ALU results
$QA0_0 \ldots QB0_0$, $F0_0 \ldots F3_0$ = the level of QA0 thru QB3 and F0 thru F3, respectively, before the indicated steady-state input conditions were established
$QA0_n \ldots QB3_n$ = the level of QA0 thru QB3 before the most recent ↑ transition of the clock
rl, ll = the level of steady-state conditions at RI/LO or LI/RO, respectively

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TYPES SN54LS690 THRU SN54LS693, SN74LS690 THRU SN74LS693

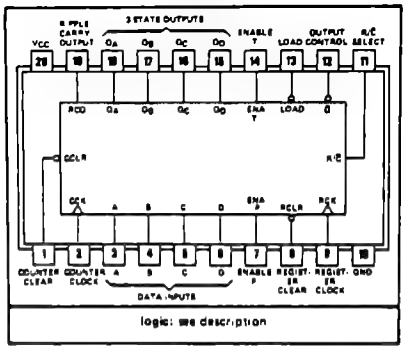
TO BE ANNOUNCED

SYNCHRONOUS COUNTERS/REGISTERS WITH MULTIPLEXED 3-STATE OUTPUTS

NOVEMBER 1977

- Replaces One SN54LS160/SN74LS160, 'LS161, 'LS162, or 'LS163, One 'LS175, and One 'LS257A in Some Applications
- Synchronously Presettable
- 3-State Outputs Drive Bus Lines Directly
- 'LS690 . . . Decade Counter, Direct Clear
- 'LS691 . . . Binary Counter, Direct Clear
- 'LS692 . . . Decade Counter, Synchronous Clear
- 'LS693 . . . Binary Counter, Synchronous Clear

SN54LS690 THRU SN54LS693 . . . . J PACKAGE
SN74LS690 THRU SN74LS693 . . . . J OR N PACKAGE
(TOP VIEW)



logic: see description

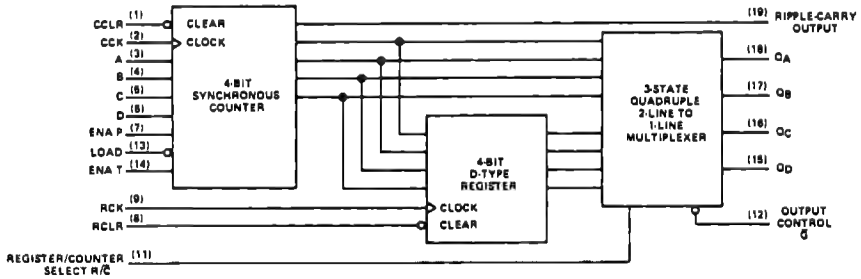
description

These low-power Schottky LSI devices incorporate synchronous counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be preset via the data inputs and have enable P and enable T inputs and a ripple-carry output for easy expansion.

The register/counter input, R/$\overline{C}$, selects the counter or register data for the four three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 millamperes and 24 millamperes for good bus-driving performance.

Individual clock and clear inputs are provided for both the counter and the latch. Both clock inputs are positive-edge triggered.

functional block diagram



TEXAS INSTRUMENTS
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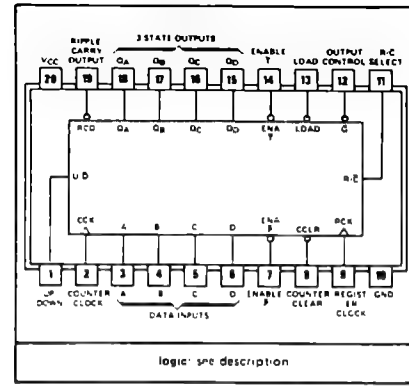
TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699
SYNCHRONOUS UP/DOWN COUNTERS/REGISTERS WITH MULTIPLEXED 3-STATE OUTPUTS

TO BE ANNOUNCED

NOVEMBER 1977

- Replaces One SN54LS168A/SN74LS168A or 'LS169A, One 'LS175, and One 'LS257A in Some Applications
- Synchronously Presettable
- 3-State Outputs Drive Bus Lines Directly
- 'LS696 . . . Decade Counter, Direct Clear
- 'LS697 . . . Binary Counter, Direct Clear
- 'LS698 . . . Decade Counter, Synchronous Clear
- 'LS699 . . . Binary Counter, Synchronous Clear

SN54LS696 THRU SN54LS699 . . . . J PACKAGE
SN74LS696 THRU SN74LS699 . . . . J OR N PACKAGE
(TOP VIEW)



logic: see description

description

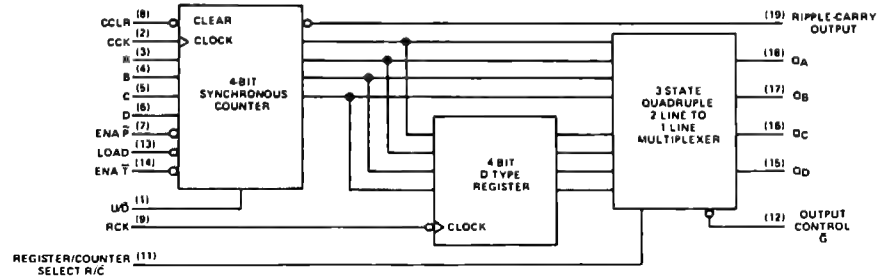
These low-power Schottky LSI devices incorporate synchronous up/down counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be preset via the data inputs and have enable $\overline{P}$ and enable $\overline{T}$ inputs and a ripple-carry output for easy expansion.

When the up/down input, U/$\overline{D}$, is high, the counter counts up, when low, it counts down.

The register/counter input, R/$\overline{C}$, selects the counter or register data for the four three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 milliamperes and 24 milliamperes for good bus-driving performance.

Individual positive-edge-triggered clocks are provided for both the up/down counter and the latch. The counter is also equipped with an active-low clear pin.

functional block diagram



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Revisions to *The TTL Data Book for Design Engineers*, Second Edition

This section contains new information and corrections for device specifications in the *"Data Book"* divided into two parts as shown below.

The reader should check the Important Notices on the back of the title page to determine the status of his data book. Second printing copies are identified by the statement "Second printing" below the copyright notice. All others are first printing.

REVISIONS TO THE FIRST PRINTING

PAGE	LOCATION	CHANGE
1-3 thru 1-8	Alphanumeric Index	1. Several types have updated specifications. Add suffix A to the type numbers listed below. 'LS73 'LS113 'LS365 'LS76 'LS114 'LS366 'LS78 'LS125 'LS367 'LS107 'LS126 'LS368 'LS112 2. Add at the end of the index: TIM9908 7-448 7-448
1-9 thru 1-28 and partially repeated 7-3 thru 7-14	Functional Index and Selection Guide	1. Add suffix A to type numbers listed above. For possible changes in selection data, see individual data sheet revisions. 2. Remove * (indicating new products) from type numbers listed below. These are now standard devices. This also applies to data sheets. 'LS147 'LS245† SN74LS362† 'LS148 'LS275 'LS373 'LS183 'LS2958 'LS374 'S226 'LS348† 'LS395A †Appears twice in index.
5-4	Absolute maximum ratings	Change "High-level voltage applied to a disabled 3-state output" from V_{CC} or 7 V to 5.5 V, for all except Series 54L/74L. Series 54L/74L has no specification.
5-6 thru 5-77	Pin assignment drawings	Add suffix A to same type numbers as in Alphanumeric Index.
5-32	107	Delete "MASTER-SLAVE" from title. Add function table for 'LS107A like that for 'LS73A on page 5-22.
5-45	168 and 170	Change SN74S168 (J, W) to SN74S168 (J, N) and SN74170 (J, W) to SN74170 (J, N)
5-50	192	Change SN74192 (J, N) second line to SN74L192 (J, N)
5-55	241 243	Re-label pin 17 to be 2A4 Change SN54243 (J, W) SN74243 (J, N) to SN54LS243 (J, W) SN74LS243 (J, N)
5-58	266	Re-label pin assignment drawing as shown below. pin 4 2Y pin 8 3A pin 5 2A pin 9 3B pin 6 2B pin 10 3Y
5-62	287 288 289	Change from SN74S287 (J, W) to SN74S287 (J, N) Change from SN74S288 (J, W) to SN74S288 (J, N) Change from SN74S289 (J, W) to SN74S289 (J, N)
5-64	299	1. Re-label pin 9 connection "CLEAR" two places. 2. Re-label pin 12 connection "CLOCK" two places.
6-25	Switching characteristics '38	Change test condition from R_L = 667 Ω to R_L = 133 Ω

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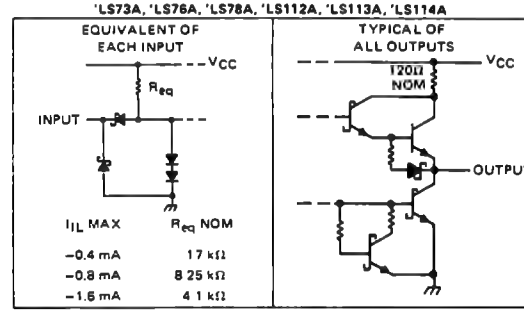
REVISIONS TO THE FIRST PRINTING

PAGE	LOCATION: AFFECTED TYPES	CHANGE
6-33	'LS125, 'LS126	Add suffix A to type numbers two places.
	Recommended operating conditions 'LS125A, 'LS126A	Change I_{OL} max limits: from to 54 FAMILY 8 mA 12 mA 74 FAMILY 16 mA 24 mA
	Electrical characteristics: 'LS125A, 'LS126A	Change test condition for V_{OL} for Series 74LS from I_{OL} = 8 mA to I_{OL} = 12 mA.
6-34	'LS125, 'LS126	Add suffix A to type numbers three places each.
	Switching characteristics: 'LS125A, 'LS126A	1. Change SN54LS/74LS test conditions to be C_L = 45 pF, R_L = 667 Ω C_L = 5 pF, R_L = 667 Ω 2. Change note to read "= Load circuit and voltage waveforms are shown on pages 3-10 and 3-11."
6-35	Schematic: 'LS125	Add suffix A to type number and add "C INPUT" to unlabeled input at left.
	Schematic: 'LS126	Add suffix A to type number and change "$\overline{G}$ INPUT" to "C INPUT."
6-36	'LS365, 'LS366 'LS367, 'LS368	Add suffix A to type numbers two places.
	Recommended operating conditions 'LS365A thru 'LS368A	Change I_{OL} maximum limits: from to SN54 FAMILY 8 mA 12 mA SN74 FAMILY 16 mA 24 mA
	Electrical characteristics: 'LS365A thru 'LS368A	Change V_{OL} test conditions to be: V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max; I_{OL} = MAX / I_{OL} = 12 mA
6-37	'LS365, 'LS366 'LS367, 'LS368	Add suffix A to type numbers.
	Schematics. '367A, '368A	[1]R is 600 Ω for the control section associated with $\overline{G}1$ and 900 Ω for the control section associated with $\overline{G}2$.
	Switching characteristics: 'LS365A thru 'LS368A	Change SN54LS/74LS test conditions: C_L = 45 pF, R_L = 667 Ω C_L = 5 pF, R_L = 667 Ω
6-38	'LS365, 'LS366 'LS367, 'LS368	Add suffix A to type numbers.

REVISIONS TO THE FIRST PRINTING

PAGE	LOCATION: AFFECTED TYPES	CHANGE
6-40	Electrical characteristics: '23, '50, '53	1. Change $I_{\overline{X}}$ maximum limit for SN7423 from −3.5 mA to −3.8 mA. 2. Change V_{OL} test conditions: from to (SN54'): $R_{\overline{X}X}$ = 138 Ω $R_{\overline{X}X}$ = ▲ (SN74'): $R_{\overline{X}X}$ = 130 Ω $R_{\overline{X}X}$ = ▲ 3. Add note "▲ $R_{\overline{X}X}$ equals 114 Ω for SN5423, 138 Ω for SN5450 and SN5453, 105 Ω for SN7423, and 130 Ω for SN7450 and SN7453."
6-43	Electrical characteristics: SN7460	Change test condition for $V_{\overline{X}X(on)}$ from $I_{\overline{X}}$ = 3.5 mA to $I_{\overline{X}}$ = 3.8 mA.
6-56	'LS73, 'LS107, 'LS113 'LS76, 'LS112, 'LS78, 'LS114	1. Add suffix A to type numbers two places. 2. Change I_{CC} maximum limit from 8 mA to 6 mA in first, third, and fourth columns only.
6-57	'LS73, 'LS76, 'LS78, 'LS107, 'LS112, 'LS113, 'LS114	1. Add suffix A to the type numbers in the switching characteristics table, the functional block diagram, and the block diagram caption. 2. Change switching characteristics: from to t_{PLH} typical 11 ns 15 ns t_{PHL} maximum 30 ns 20 ns 3. Change schematics as shown below. 'LS73A, 'LS76A, 'LS78A, 'LS112A, 'LS113A, 'LS114A 
6-61	Switching characteristics: '279, 'LS279	1. Label existing limits column for '279 2. Add new column shown: 'LS279: MIN — TYP 12, 13, 15 — MAX 22, 21, 27
6-69	Equivalent input: 'LS221	Delete "25 kΩ NOM" and replace with "R_{eq}".

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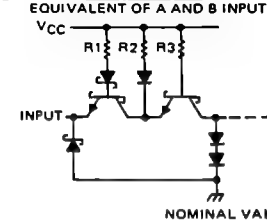
REVISIONS TO THE FIRST PRINTING

<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>6-71</td><td>Recommended operating conditions: 'LS221</td><td>Change "Output duty cycle " maximum limits for R_T = 2 kΩ from 67% to 50%.</td></tr>
<tr><td></td><td>Electrical characteristics: 'LS221</td><td>Change I_{IL} maximum limit for Input B from −0.4 mA to −0.8 mA.</td></tr>
<tr><td>6-83</td><td>'LS241, 'S241</td><td>Relabel pin 17 "2A4" in pin assignment drawing.</td></tr>
<tr><td>6-84</td><td>Electrical characteristics: 'LS240, 'LS241, 'LS244</td><td>1. Change V_{OH} test conditions to be:
V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −3 mA
V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX
2. Change I_{OS} minimum limit from −50 mA to −40 mA two places.</td></tr>
<tr><td>6-85</td><td>Electrical characteristics: SN74S240, SN74S241</td><td>Add a set of test conditions and limits for V_{OH} and label existing conditions as shown below.
<table>
<tr><th></th><th></th><th colspan="3">MIN TYP MAX</th><th colspan="3">MIN TYP MAX</th><th>UNIT</th></tr>
<tr><td>SN74S'</td><td>V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA</td><td colspan="3">2.7</td><td colspan="3">2.7</td><td rowspan="3">V</td></tr>
<tr><td>SN54S' and SN74S'</td><td>V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −3 mA</td><td colspan="3">2.4 3.4</td><td colspan="3">2.4 3.4</td></tr>
<tr><td>SN54S' and SN74S'</td><td>V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX</td><td colspan="3">2</td><td colspan="3">2</td></tr>
</table></td></tr>
<tr><td>6-88</td><td>Electrical characteristics: 'LS242, 'LS243</td><td>1. Change I_{OZH} maximum limit from 20 μA to 40 μA two places.
2. Add a set of test conditions and limits for I_I as shown below.
<table>
<tr><th></th><th></th><th></th><th colspan="3">MIN TYP MAX</th><th colspan="3">MIN TYP MAX</th><th>UNIT</th></tr>
<tr><td>A or B</td><td rowspan="2">V_{CC} = MAX</td><td>V_I = 5.5 V</td><td colspan="3">0.1</td><td colspan="3">0.1</td><td rowspan="2">mA</td></tr>
<tr><td>$\overline{G}$AB or $\overline{G}$BA</td><td>V_I = 7 V</td><td colspan="3">0.1</td><td colspan="3">0.1</td></tr>
</table>
3. Change I_{OS} minimum limit from −50 mA to −40 mA two places.</td></tr>
<tr><td>6-98</td><td>Figure 10, Note B. Expandable gates</td><td>Delete the parenthetic statement regarding resistor values and add the table below.
<table>
<tr><th colspan="2">RESISTANCE VALUE TABLE</th></tr>
<tr><td>SN5423</td><td>114 Ω</td></tr>
<tr><td>SN5450, SN5453</td><td>138 Ω</td></tr>
<tr><td>SN7423</td><td>105 Ω</td></tr>
<tr><td>SN7450, SN7453</td><td>130 Ω</td></tr>
</table></td></tr>
</table>

REVISIONS TO THE FIRST PRINTING

<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-74</td><td>'LS90, 'LS92, 'LS93</td><td>Delete Schottky diode in parallel with input transistor.

'LS90, 'LS92, 'LS93
EQUIVALENT OF A AND B INPUTS
 

NOMINAL VALUES
<table>
<tr><th>INPUT</th><th>R1</th><th>R2</th><th>R3</th></tr>
<tr><td>A</td><td>10 kΩ</td><td>10 kΩ</td><td>10 kΩ</td></tr>
<tr><td>B ('LS90, 'LS92)</td><td>6.7 kΩ</td><td>6.7 kΩ</td><td>5 kΩ</td></tr>
<tr><td>B ('LS93)</td><td>15 kΩ</td><td>15 kΩ</td><td>10 kΩ</td></tr>
</table></td></tr>
<tr><td>7-78</td><td>Electrical characteristics: 'LS90, 'LS92</td><td>1. Change I_{IL} "output current" to "input current".
2. Change note to be "Q_A outputs are tested . . ."</td></tr>
<tr><td>7-79</td><td>Electrical characteristics, 'LS93</td><td>Change I_{IL} "output current" to "input current"</td></tr>
<tr><td>7-100</td><td>Recommended operating conditions, 'LS96</td><td>Change "width of clock pulse, $t_{w(clock)}$" minimum limit from 35 ns to 20 ns.</td></tr>
<tr><td>7-123</td><td>Description: 'LS124, 'S124</td><td>Delete the last sentence of the fourth paragraph under description, "Simultaneous operation . . . not recommended."</td></tr>
<tr><td rowspan="3">7-155</td><td>Electrical characteristics: 'LS147, 'LS148</td><td>Change SN54LS', SN74LS' maximum V_{OH} limits to minimum limits.</td></tr>
<tr><td>Switching characteristics: 'LS147</td><td>Change 'LS147 limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>12</td><td>18</td></tr>
<tr><td></td><td>12</td><td>18</td></tr>
<tr><td></td><td>21</td><td>33</td></tr>
<tr><td></td><td>15</td><td>23</td></tr>
</table></td></tr>
<tr><td>Switching characteristics: 'LS148</td><td>Change 'LS148 limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>14</td><td>18</td></tr>
<tr><td></td><td>15</td><td>25</td></tr>
<tr><td></td><td>20</td><td>36</td></tr>
<tr><td></td><td>16</td><td>29</td></tr>
<tr><td></td><td>7</td><td>18</td></tr>
<tr><td></td><td>25</td><td>40</td></tr>
<tr><td></td><td>35</td><td>55</td></tr>
<tr><td></td><td>9</td><td>21</td></tr>
<tr><td></td><td>16</td><td>25</td></tr>
<tr><td></td><td>12</td><td>25</td></tr>
<tr><td></td><td>12</td><td>17</td></tr>
<tr><td></td><td>14</td><td>38</td></tr>
<tr><td></td><td>12</td><td>21</td></tr>
<tr><td></td><td>23</td><td>35</td></tr>
</table></td></tr>
</table>

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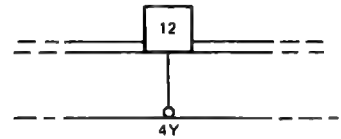
<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-177</td><td>Electrical characteristics
'155</td><td>Change V_{IK} test conditions from $I_I = -12$ mA to $I_I = -8$ mA.</td></tr>
<tr><td>7-179</td><td>Electrical characteristics
'156</td><td>Change V_{IK} test conditions from $I_I = -12$ mA to $I_I = -8$ mA.</td></tr>
<tr><td>7-181</td><td>Pin assignment drawing:
'LS158, 'S158</td><td>Add inversion indicator for output 4Y.
 
</td></tr>
<tr><td>7-187</td><td>Electrical characteristics:
'S157, 'S158</td><td>1. Change Note 2 to read "I_{CC} is measured with all outputs open".
2. Change I_{CC} test conditions and limits columns to be:
<table>
<tr><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>V_{CC} = MAX, All inputs at 4.5 V, See Note 2</td><td></td><td>50</td><td>78</td><td></td><td>39</td><td>61</td><td rowspan="2">mA</td></tr>
<tr><td>V_{CC} = MAX, A Inputs at 4.5 V, B, G, S Inputs at 0 V, See Note 2</td><td></td><td></td><td></td><td></td><td></td><td>81</td></tr>
</table></td></tr>
<tr><td>7-190</td><td>Description:
'160 thru '163,
'LS160A thru 'LS163A,
'S162, 'S163</td><td>Change third and fourth sentences of second paragraph to read: "Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163."</td></tr>
<tr><td>7-200</td><td>Equivalent schematic of each input:
'S162, 'S163</td><td>Add a 20-kΩ resistor between V_{CC} and input for all inputs except clock and load.
Clock and load inputs have no such resistor.</td></tr>
<tr><td>7-219</td><td>Notes: '166</td><td>1. Change present Note 2 to Note 3.
2. Add new Note 2: An SN54166 in the W package operating at free-air temperatures above 113°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.</td></tr>
<tr><td></td><td>Absolute maximum ratings: SN54166</td><td>Add "(see Note 2)" to "Operating free-air temperature range: SN54166."</td></tr>
<tr><td></td><td>Recommended operating conditions: SN54166</td><td>Add "(see Note 2)" to "Operating free-air temperature range, T_A."</td></tr>
<tr><td></td><td>Electrical characteristics:
'166</td><td>1. Change I_{CC} test condition from "See Note 2" to "See Note 3."
2. Change I_{CC} values as shown:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>90</td><td>127</td><td></td><td>90</td><td>127</td></tr>
</table></td></tr>
</table>

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PAGE	LOCATION: AFFECTED TYPES	CHANGE
7-220	Electrical characteristics: 'LS166	Change "Note 2" to "Note 3" for I_{CC} test conditions and in notes.
7-227	Block Diagram, 'LS169A	Change the AND gate for Ripple Carry output, Pin 15, to a NAND gate.
7-233	Equivalent schematic of each input: 'S168, 'S169	Add a 20-kΩ resistor between V_{CC} and the Input for Load input only. All other inputs have no such resistor.
7-286	Typical application data: '182, 'S182	Change " '181 or 'S182" to " '182 or 'S182".
7-288	Electrical characteristics: 'H183	1. Add I_{CCH} maximum limit of 65 mA. 2. Change Note 4 ". . . and all outputs at 4.5 V" to ". . . and all inputs at 4.5 V".
7-289	Note 4: 'LS183	Change Note 4 " and all outputs at 4.5 V." to ". . . and all inputs at 4.5 V".
	Switching characteristics: 'LS183	Change limits column to be:

MIN	TYP	MAX
	9	15
	20	33

PAGE	LOCATION: AFFECTED TYPES	CHANGE
7-302	Recommended operating conditions: 'LS190, 'LS191	Change minimum limit for "Count enable time, t_{enable}" from 20 ns to 40 ns two places.
7-306	Description: '192, '193, 'L192, 'L193, 'LS192, 'LS193	Change ". . . count-down input" in the next-to-last line to ". . . count-up input".
7-313	Recommended operating conditions: 'LS192, 'LS193	Add parameter "Clear inactive-state setup time, t_{su}" with minimum limit of 40 ns for SN54LS' and SN74LS'.
	Switching characteristics: 'LS142, 'LS143	Change limits column to be:

MIN	TYP	MAX
25	32	
	17	26
	18	24
	16	24
	15	24
	27	38
	30	47
	24	40
	26	40
	23	35

PAGE	LOCATION: AFFECTED TYPES	CHANGE
7-332	Recommended operating conditions: '196, '197	Change "Pulse width, t_w" Clock-1 input minimum limit from 20 ns to 10 ns two places, and Clock-2 input minimum limit from 30 ns to 20 ns two places.
7-334	Recommended operating conditions. 'LS196, 'LS197	Change "Count enable time, t_{enable}" minimum limit from 20 ns to 30 ns two places.

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<table>
<tr><th>PAGE</th><th>LOCATION
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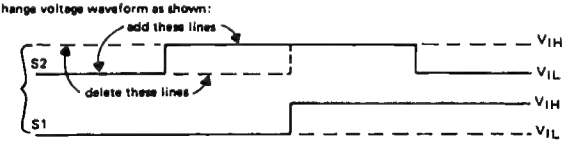
<tr><td>7-343</td><td>Electrical characteristics:
'198, '199</td><td>Change limits columns for I_{CC} to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td></td><td>90</td><td>127</td><td></td><td>90</td><td>127</td><td>mA</td></tr>
</table></td></tr>
<tr><td>7-346</td><td>Function tables:
'S226</td><td>Modify the first two lines to make the table read:
BUS-MANAGEMENT FUNCTION TABLE
<table>
<tr><th>OPERATION</th><th>S2</th><th>S1</th><th>LATCH FUNCTIONS</th></tr>
<tr><td>DRIVE BUS A</td><td>L</td><td>L</td><td>Pass Bus B Data to Bus A</td></tr>
<tr><td>DRIVE BUS B</td><td>H</td><td>L</td><td>Pass Bus A Data to Bus B</td></tr>
<tr><td>EXCHANGE</td><td>H</td><td>H</td><td>Store Bus A and Bus B Data</td></tr>
<tr><td>BUS A AND B</td><td>L</td><td>H</td><td>Read Out Stored Data</td></tr>
</table></td></tr>
<tr><td></td><td>Absolute maximum ratings:
SN54S226</td><td>1. Change operating temperature specification to be:
Operating free-air temperature range: SN54S226 (see Note 2) . . .
2. Add "NOTE 2: An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W."</td></tr>
<tr><td>7-347</td><td>Recommended operating conditions: 'S226</td><td>1. Change minimum limit for "Data setup time, t_{su}" from 5↓ to 0↓ four places.
2. Change minimum limit for "Data hold time, t_h" from 5↓ to 3↓ four places.
3. Add (see Note 2) to "Operating free-air temperature, T_A".</td></tr>
<tr><td></td><td>Electrical characteristics:
'S226</td><td>1. Change present Note 2 to Note 3 and add new Note 2 same as page 7-346.
2. Change I_{CC} test conditions from "See Note 2" to "See Note 3" and add a maximum limit of 185 mA.
3. Change I_{IL} maximum limit from −300 μA to −380 μA.</td></tr>
<tr><td>7-348</td><td>Switching characteristics:
'S226</td><td>Change table as shown:
<table>
<tr><th>TEST CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td rowspan="8">C_L = 50 pF, R_L = 280 Ω,
See Note 4</td><td></td><td>20</td><td>30</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>15</td><td>30</td></tr>
<tr><td></td><td>25</td><td>37</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>19</td><td>30</td></tr>
<tr><td></td><td>25</td><td>37</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>19</td><td>30</td></tr>
<tr><td></td><td>12</td><td>20</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>12</td><td>20</td></tr>
<tr><td rowspan="2">C_L = 5 pF, R_L = 280 Ω,
See Note 4</td><td></td><td>10</td><td>15</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>10</td><td>15</td></tr>
</table></td></tr>
<tr><td></td><td>Notes: 'S226</td><td>Change present Note 2 to Note 4.</td></tr>
<tr><td></td><td>Applications:
'S226</td><td>Change voltage waveform as shown:

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<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-349</td><td>Features, 'LS245</td><td>• Typical Propagation Delay Times, Port-to-Port . . . 8 ns</td></tr>
<tr><td>7-350</td><td>Electrical characteristics:
'LS245</td><td>1. Change limits columns for parameters shown.
<table>
<tr><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>I_{OZH}</td><td></td><td></td><td>10</td><td></td><td></td><td>10</td><td rowspan="2">μA</td></tr>
<tr><td>I_{OZL}</td><td></td><td></td><td>−200</td><td></td><td></td><td>−200</td></tr>
<tr><td rowspan="3">I_{CC}</td><td></td><td>48</td><td>70</td><td></td><td>48</td><td>70</td><td rowspan="3">mA</td></tr>
<tr><td></td><td>62</td><td>90</td><td></td><td>62</td><td>90</td></tr>
<tr><td></td><td>64</td><td>95</td><td></td><td>64</td><td>95</td></tr>
</table>
2. Change I_I test conditions and limits as shown below.
<table>
<tr><td>A or B
DIR or $\overline{G}$</td><td>V_{CC} = MAX</td><td>V_I = 5.5 V
V_I = 7 V</td><td>0.1
0.1</td><td>0.1
0.1</td><td>mA</td></tr>
</table></td></tr>
<tr><td></td><td>Switching characteristics:
'LS245</td><td>Change limits column to be.
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>8</td><td>12</td></tr>
<tr><td></td><td>8</td><td>12</td></tr>
<tr><td></td><td>27</td><td>40</td></tr>
<tr><td></td><td>25</td><td>40</td></tr>
<tr><td></td><td>15</td><td>25</td></tr>
<tr><td></td><td>15</td><td>25</td></tr>
</table></td></tr>
<tr><td>7-374</td><td>Electrical characteristics:
'LS257, 'LS258</td><td>Change I_{OZH} test condition from V_O = 2.4 V to V_O = 2.7 V</td></tr>
<tr><td></td><td>Switching characteristics:
'LS257, 'LS258</td><td>Change R_L = 667 kΩ to R_L = 667 Ω</td></tr>
<tr><td>7-375</td><td>Electrical characteristics:
'S257, 'S258</td><td>Add to V_{OH} new test conditions and limits as shown.
<table>
<tr><th></th><th></th><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>V_{CC} = MIN, V_{IH} = 2 V,
V_{IL} = 0.8 V, I_{OH} = −1 mA</td><td></td><td>SN74S'</td><td>2.7</td><td></td><td></td><td>2.7</td><td></td><td></td><td>V</td></tr>
</table></td></tr>
<tr><td>7-393</td><td>Switching characteristics:
'LS275</td><td>Change test conditions and limits columns as shown.
<table>
<tr><th></th><th></th><th></th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td>Any</td><td>C_L = 45 pF, R_L = 667 Ω,
See Note 2</td><td></td><td>35
42</td><td>62
66</td></tr>
<tr><td>Enable $\overline{G}$</td><td>Any</td><td>C_L = 45 pF, R_L = 667 Ω,
See Note 2
C_L = 5 pF, R_L = 667 Ω,
See Note 2</td><td></td><td>8
13
10
10</td><td>23
23
15
15</td></tr>
</table></td></tr>
<tr><td>7-407</td><td>Electrical characteristics:
SN54LS280</td><td>Change I_{CC} minimum value for SN54LS280 to a typical value (16 mA).</td></tr>
</table>

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<table>
<tr><th>PAGE</th><th>LOCATION:
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<tr><td>7-426</td><td>Electrical characteristics:
'290, '293</td><td>Change I_{IL} "High-level input . . ." to "Low-level input . . ."</td></tr>
<tr><td></td><td>Switching characteristics:
'290</td><td>Change t_{PHL} maximum limit, bottom line, from 24 ns to 40 ns.</td></tr>
<tr><td>7-428</td><td>Electrical characteristics:
'LS290, 'LS293</td><td>Change I_{IL} "Low-level output . . ." to "Low-level input . . ."</td></tr>
<tr><td>7-430</td><td>Electrical characteristics:
'2958</td><td>Change I_{CC} limits columns to be.
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td></td><td>20</td><td>29</td><td></td><td>20</td><td>29</td><td rowspan="2">mA</td></tr>
<tr><td></td><td>22</td><td>33</td><td></td><td>22</td><td>33</td></tr>
</table></td></tr>
<tr><td>7-431</td><td>Switching characteristics:
'LS295B</td><td>Change limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td>30</td><td>45</td><td></td></tr>
<tr><td></td><td>14</td><td>20</td></tr>
<tr><td></td><td>19</td><td>30</td></tr>
<tr><td></td><td>18</td><td>26</td></tr>
<tr><td></td><td>20</td><td>30</td></tr>
<tr><td></td><td>13</td><td>20</td></tr>
<tr><td></td><td>13</td><td>20</td></tr>
</table></td></tr>
<tr><td>7-440</td><td>Electrical characteristics:
'LS209</td><td>1. Change I_I as shown below.
<table>
<tr><th></th><th></th><th></th><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>S0, S1</td><td rowspan="3">V_{CC} = MAX</td><td>V_I = 7 V</td><td></td><td></td><td>200</td><td></td><td></td><td>200</td><td rowspan="3">μA</td></tr>
<tr><td>A thru H</td><td>V_I = 5.5 V</td><td></td><td></td><td>100</td><td></td><td></td><td>100</td></tr>
<tr><td>Any other</td><td>V_I = 7 V</td><td></td><td></td><td>100</td><td></td><td></td><td>100</td></tr>
</table>
2. Change I_{IH} maximum limit for "Any other" input from 30 μA to 20 μA two places.
3. Change I_{IL} test condition from V_I = 0.5 V to V_I = 0.4 V.</td></tr>
<tr><td>7-449</td><td>Electrical characteristics:
'LS348</td><td>Add I_{OZ} for A0, A1, and A2 outputs exactly like that for the 'LS353 on page 7-459.</td></tr>
<tr><td>7-450</td><td>Switching characteristics:
'LS348
(TIM9908)</td><td>Change test conditions and limits column as shown below.
<table>
<tr><th>TEST CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td rowspan="2">C_L = 45 pF,
R_L = 667 Ω,
See Note 3</td><td></td><td>11</td><td>17</td><td>ns</td></tr>
<tr><td></td><td>20</td><td>30</td><td></td></tr>
<tr><td rowspan="2">C_L = 15 pF,
R_L = 2 kΩ,
See Note 3</td><td></td><td>23</td><td>35</td><td>ns</td></tr>
<tr><td></td><td>23</td><td>35</td><td></td></tr>
<tr><td rowspan="8">C_L = 15 pF,
R_L = 2 kΩ,
See Note 3</td><td></td><td>11</td><td>18</td><td>ns</td></tr>
<tr><td></td><td>26</td><td>40</td><td></td></tr>
<tr><td></td><td>38</td><td>55</td><td>ns</td></tr>
<tr><td></td><td>9</td><td>21</td><td></td></tr>
<tr><td></td><td>11</td><td>17</td><td>ns</td></tr>
<tr><td></td><td>14</td><td>36</td><td></td></tr>
<tr><td></td><td>17</td><td>21</td><td>ns</td></tr>
<tr><td></td><td>25</td><td>40</td><td></td></tr>
<tr><td rowspan="2">C_L = 45 pF, R_L = 667 Ω,
See Note 3</td><td></td><td>25</td><td>39</td><td>ns</td></tr>
<tr><td></td><td>24</td><td>41</td><td></td></tr>
<tr><td rowspan="2">C_L = 5 pF,
R_L = 667 Ω</td><td></td><td>18</td><td>27</td><td>ns</td></tr>
<tr><td></td><td>23</td><td>35</td><td></td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>PAGE</th><th>LOCATION:
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<tr><td>7-453</td><td>Switching characteristics:
'351</td><td>Add maximum values and change one typical value as shown below.
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td></td><td>20</td><td>30</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>20</td><td>30</td></tr>
<tr><td></td><td>10</td><td>22</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>10</td><td>22</td></tr>
<tr><td></td><td>18</td><td>33</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>20</td><td>33</td></tr>
<tr><td></td><td>8</td><td>20</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>10</td><td>20</td></tr>
</table></td></tr>
<tr><td>7-463</td><td>Switching characteristics:
'LS362 (TIM9904)</td><td>1. Change V_{CC1} to V_{CC} and V_{CC2} to V_{DD}.
2. Change minimum limits for $t_{f(e)}$ and $t_{f(o)}$ from 10 ns to 5 ns.</td></tr>
<tr><td>7-474</td><td>Electrical characteristics:
'LS374</td><td>Change I_{CC} maximum limit for 'LS374 from 45 mA to 40 mA two places.</td></tr>
<tr><td></td><td>Switching characteristics:
'LS373, 'LS374</td><td>Change limits columns to be:
<table>
<tr><th colspan="3">'LS373</th><th colspan="3">'LS374</th></tr>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td></td><td></td><td></td><td></td><td>35</td><td>50</td></tr>
<tr><td></td><td>12</td><td>18</td><td></td><td></td><td></td></tr>
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<tr><td></td><td>20</td><td>30</td><td></td><td>15</td><td>28</td></tr>
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<tr><td></td><td>15</td><td>25</td><td></td><td>14</td><td>25</td></tr>
</table></td></tr>
<tr><td>7-485</td><td>Functional block
diagram: 'S381</td><td>Add one input to the $\overline{P}$ gate and connect to C_n input.</td></tr>
<tr><td>7-497</td><td>Electrical characteristics:
'S395A</td><td>Change limits columns for I_{CC} as shown.
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td>22</td><td>34</td><td></td><td>22</td><td>34</td></tr>
<tr><td>21</td><td>31</td><td></td><td>21</td><td>31</td></tr>
</table></td></tr>
<tr><td>7-498</td><td>Switching characteristics:
'LS395</td><td>Change limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td>30</td><td>45</td><td></td></tr>
<tr><td></td><td>22</td><td>35</td></tr>
<tr><td></td><td>15</td><td>30</td></tr>
<tr><td></td><td>20</td><td>30</td></tr>
<tr><td></td><td>15</td><td>25</td></tr>
<tr><td></td><td>17</td><td>25</td></tr>
<tr><td></td><td>11</td><td>17</td></tr>
<tr><td></td><td>12</td><td>20</td></tr>
</table></td></tr>
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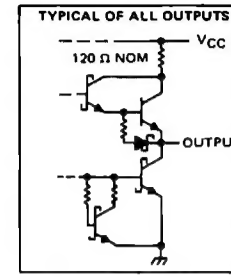
<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td rowspan="2">7-510</td><td>Switching characteristics:
SN74LS424 (TIM8224)</td><td>1. Change minimum limit for $t_{\phi 2L,\phi 1H}$ to be $\frac{2t_c}{9} - 30$ ns.
2. Change minimum limit for $t_{\phi 2H,SSL}$ to be $\frac{6t_c}{9} - 50$ ns.</td></tr>
<tr><td>Example:
SN74LS424 (TIM8224)</td><td>1. Change minimum limit for $t_{\phi 2L,\phi 1H}$ from 86 ns to 70 ns.
2. Change minimum limit for $t_{\phi 2H,SSL}$ from 270 ns to 250 ns.</td></tr>
<tr><td>7-513</td><td>Figure 6:
SN74LS424 (TIM8224)</td><td>Add applications information shown below.
CRYSTAL REQUIREMENTS
Frequency tolerance: ±0.005% for 0°C to 70°C
Resonance Mode: series, fundamental (use 3rd overtone mode with tank circuit
Load capacitance: 20 pF to 35 pF
Equivalent resistance: 20 Ω to 75 Ω
Minimum power dissipation: 4 mW</td></tr>
<tr><td>7-529</td><td>Switching characteristics:
'LS670</td><td>1. Change table as shown below for the bottom four parameters.
<table>
<tr><td>t_{PZH}</td><td rowspan="4">Read enable</td><td rowspan="4">Any Q</td><td>C_L = 15 pF, R_L = 2 kΩ,
See Figures 1 and 4</td></tr>
<tr><td>t_{PZL}</td></tr>
<tr><td>t_{PHZ}</td><td rowspan="2">C_L = 5 pF, R_L = 2 kΩ,
See Figures 1 and 4</td></tr>
<tr><td>t_{PLZ}</td></tr>
</table>
2. Change enable time and disable time symbols shown below for definitions.
<table>
<tr><th>from</th><th>to</th></tr>
<tr><td>t_{ZH}</td><td>t_{PZH}</td></tr>
<tr><td>t_{ZL}</td><td>t_{PZL}</td></tr>
<tr><td>t_{HZ}</td><td>t_{PHZ}</td></tr>
<tr><td>t_{LZ}</td><td>t_{PLZ}</td></tr>
</table></td></tr>
</table>

REVISIONS TO THE FIRST AND SECOND PRINTINGS

<table>
<tr><th>PAGE</th><th>LOCATION:
AFFECTED TYPES</th><th>CHANGE</th></tr>
<tr><td>7-153</td><td>Output schematic:
'LS147, 'LS148</td><td>Add a Schottky diode as shown.
 
</td></tr>
<tr><td rowspan="2">7-440</td><td>Electrical characteristics:
'LS299</td><td>1. Change V_{OH} minimum limit for SN54LS299 for "Q_A" or "Q_H'" from 2.7 V to 2.5 V.
2. Change I_{CC} typical and maximum from 35 mA and 60 mA to 33 mA and 53 mA respectively.</td></tr>
<tr><td>Switching characteristics
'LS299</td><td>Change limits column to be:
<table>
<tr><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>35</td><td>50</td><td></td><td>MHZ</td></tr>
<tr><td></td><td>22</td><td>33</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>26</td><td>39</td></tr>
<tr><td></td><td>27</td><td>40</td><td>ns</td></tr>
<tr><td></td><td>17</td><td>25</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>26</td><td>39</td></tr>
<tr><td></td><td>26</td><td>40</td><td>ns</td></tr>
<tr><td></td><td>13</td><td>21</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>19</td><td>30</td></tr>
<tr><td></td><td>10</td><td>15</td><td rowspan="2">ns</td></tr>
<tr><td></td><td>10</td><td>15</td></tr>
</table></td></tr>
<tr><td>7-494</td><td>Electrical characteristics:
'LS390, 'LS393</td><td>1. Change I_{IH} maximum limit for Input A from 40 μA to 100 μA two places.
2. Change I_{IH} maximum limit for Input B from 80 μA to 200 μA two places.</td></tr>
<tr><td>7-524</td><td>Electrical characteristics:
'LS490</td><td>1. Change V_{IK} test condition from I_I = −1 mA to I_I = −18 mA.
2. Change I_{IH} maximum limit for "Clock" from 40 μA to 100 μA.</td></tr>
</table>

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